3A6000

龙 龙 芯

V1.2

2024 07

Loongson Technology Corporation Limited
Building No.2, Loongson Industrial Park,
Zhongguancun Environmental Protection Park, Haidian District, Beijing
(Tel) 010-62546668
(Fax) 010-62600826

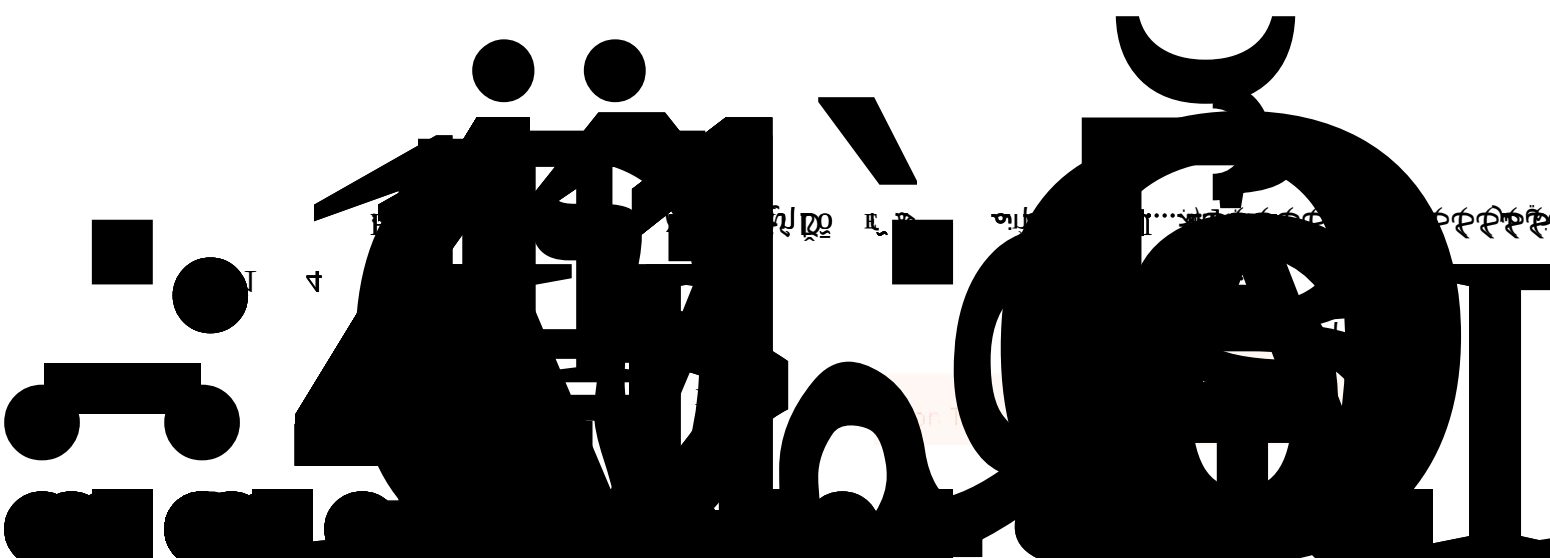
كج كج 3A6000 ´Y كج كج 3A6000

شجـ w كج ↓ آ

3A6000 ಕ್ ಕ್ ಗೆ

11- 4

.



3A6000 ಶ್ರ ಶ್ರ

1

1.1

ر ´ ↓ 1 ↓ ر 32 ر ٰ

ﻣ o h ١ =

ر

2 ↓ ر 32 64 ر ٰ ﻣ o h

L w SoC 3 ↓ ر ṗ

64 ر ă ḍ

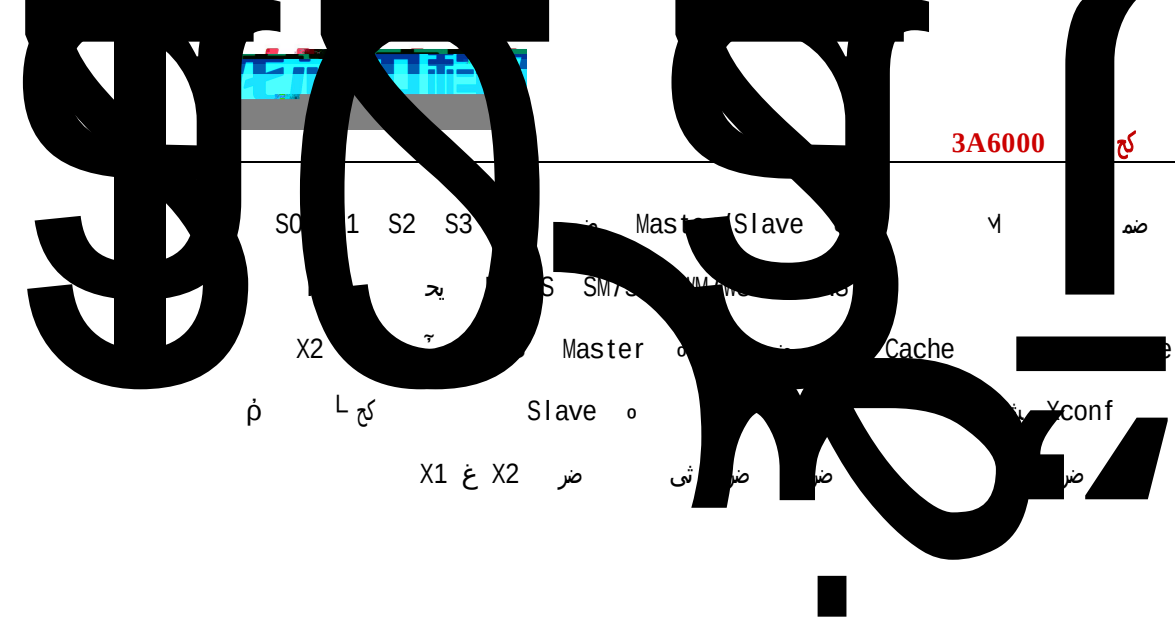
S0 1 S2 S3 Mast Slave ٧ ضم h أ

يح S SM7

X2 Master Cache ه ٥

ṕ كج L Slave ٥ Yconf شج

ضر ضر ضر ضر X2 غ X1



5x5 ĩ ˜ ضم كح ضم ¨ Cache شجـ ĩ

IO ٥ IO-RING

5x3 ĩ ˜ 4 ¨ Cache شجـ DDR4 ṗ ˪ كح

ĩ IO ٥ IO-RING

IO-RING´ ƈ ٥ ´ HT ˪ كح MISC شجـ SE شجـ ĩ ˜ HT

˪ كح ṗ DMA ˪ كح DMA ˪ كح IO DMA ˪

Ω№ 128 ضي كح

 ĩ ˜ 4 كح

scache 256 ṗ كح scache

2

2.1

3A6000 ヽ 4 8

2.2

L ´ DO_TEST CHIP_CONFIG[9:0]

2- 1 L

~	
DO_TEST	1 ' b1 w 1 ' b0

]

CHIP_CONFIG[9:4]

3

خي . ̂ №خي ضر كج ↓ 3̂

خي ضر 4 خي ضر 48 خي ضر ا Ũ

خي ضر 44 № ا ⌡ 16 № ~شخ

خي ضر № ₹ خي ضر 44 ا ٦ ´ ٦ 3A6000

3.1

3A6000 ا 4 8

4'h3	13:12	4'hb	29:28
4'h4	15:14	4'hc	31:30
4'h5	17:16	4'hd	33:32
4'h6	19:18	4'he	35:34
4'h7	21:20	4'hf	37:36

3A6000 كج ṗ 44 خي ضر № ĩ MC interleave خي ضر IOCSR[0x400] =

3- 3 ṗ 44 خي ضر№

مخ خي ضر		ضر
addr[43:40]==4 ' hc	ضر ,uncache	SE
addr[43:40]==4 ' he	ضر ,uncache	HT
0x10000000-0x1fffffff, 0x3ff00000-0x3ff0ffff(˜)	ضر ,uncache	MISC
Mc interleave 0 خي ضر	ضر ,uncache	MC0
Mc interleave 1 خي ضر	ضر ,uncache	MC1
Scache interleave 0(scid_sel _ خي ضر)	ضر ,cache	Scache0
Scache interleave 1(scid_sel _ خي ضر)	ضر ,cache	Scache1
Scache interleave 2(scid_sel _ خي ضر)	ضر ,cache	Scache2
Scache interleave 3(scid_sel _ خي ضر)	ضر ,cache	Scache3

3.2

3A6000 ĩ ˜ IO-RING ˜

Master o ⌠ Master o 8 خي ضر o ˜

8 خي ضر o خي ضر o BASE MASK غ MMAP 64 كج

BASE K MASK 1 MMAP ضم

Slave o ˜ MMAP[4] ŭ MMAP[5] شج MMAP[6]

MMAP[7] o

3- 4 MMAP

[7]	[6]	[5]	[4]
o	SCACHE/ ṗ	شج	ŭ

o ث : (IN_ADDR & MASK) == BASE

3˜ نه ضي Ω¯ o ˜

ì

SCACHE/ ṗ U Slave˝ 0 4 0 ⌈

SCACHE SCID_SEL _ ضي 4 SCACHE 4 ⌈ ṗ

interleave_bit _ ضي 2 MC

خي ضر o كح خي ضر 0x1FE0_0000 IOCSR

كح o خي ضر 5 -3

خي ضر	كح	خي ضر	كح
0x2000	CORE0_WIN0_BASE	0x2100	CORE1_WIN0_BASE
0x2008	CORE0_WIN1_BASE	0x2108	CORE1_WIN1_BASE
0x2010	CORE0_WIN2_BASE	0x2110	CORE1_WIN2_BASE
0x2018	CORE0_WIN3_BASE	0x2118	CORE1_WIN3_BASE
0x2020	CORE0_WIN4_BASE	0x2120	CORE1_WIN4_BASE
0x2028	CORE0_WIN5_BASE	0x2128	CORE1_WIN5_BASE
0x2030	CORE0_WIN6_BASE	0x2130	CORE1_WIN6_BASE
0x2038	CORE0_WIN7_BASE	0x2138	CORE1_WIN7_BASE
0x2040	CORE0_WIN0_MASK		

0x2238	CORE2_WIN7_BASE	0x2338	CORE3_WIN7_BASE
0x2240	CORE2_WIN0_MASK	0x2340	CORE3_WIN0_MASK
0x2248	CORE2_WIN1_MASK	0x2348	CORE3_WIN1_MASK
0x2250	CORE2_WIN2_MASK	0x2350	CORE3_WIN2_MASK
0x2258	CORE2_WIN3_MASK	0x2358	CORE3_WIN3_MASK
0x2260	CORE2_WIN4_MASK	0x2360	CORE3_WIN4_MASK
0x2268	CORE2_WIN5_MASK	0x2368	CORE3_WIN5_MASK
0x2270	CORE2_WIN6_MASK	0x2370	CORE3_WIN6_MASK
0x2278	CORE2_WIN7_MASK	0x2378	CORE3_WIN7_MASK
0x2280	CORE2_WIN0_MMAP	0x2380	CORE3_WIN0_MMAP
0x2288	CORE2_WIN1_MMAP	0x2388	CORE3_WIN1_MMAP
0x2290	CORE2_WIN2_MMAP	0x2390	CORE3_WIN2_MMAP
0x2298	CORE2_WIN3_MMAP	0x2398	CORE3_WIN3_MMAP
0x22a0	CORE2_WIN4_MMAP	0x23a0	CORE3_WIN4_MMAP
0x22a8	CORE2_WIN5_MMAP	0x23a8	CORE3_WIN5_MMAP
0x22b0	CORE2_WIN6_MMAP	0x23b0	CORE3_WIN6_MMAP
0x22b8	CORE2_WIN7_MMAP	0x23b8	CORE3_WIN7_MMAP
0x2400	SCACHE0_WIN0_BASE	0x2500	SCACHE1_WIN0_BASE
0x2408	SCACHE0_WIN1_BASE	0x2508	SCACHE1_WIN1_BASE
0x2410	SCACHE0_WIN2_BASE	0x2510	SCACHE1_WIN2_BASE
0x2418	SCACHE0_WIN3_BASE	0x2518	SCACHE1_WIN3_BASE
0x2420	SCACHE0_WIN4_BASE	0x2520	SCACHE1_WIN4_BASE
0x2428	SCACHE0_WIN5_BASE	0x2528	SCACHE1_WIN5_BASE
0x2430	SCACHE0_WIN6_BASE	0x2530	SCACHE1_WIN6_BASE
0x2438	SCACHE0_WIN7_BASE	0x2538	SCACHE1_WIN7_BASE
0x2440	SCACHE0_WIN0_MASK	0x2540	SCACHE1_WIN0_MASK
0x2448	SCACHE0_WIN1_MASK	0x2548	SCACHE1_WIN1_MASK
0x2450	SCACHE0_WIN2_MASK	0x2550	SCACHE1_WIN2_MASK
0x2458	SCACHE0_WIN3_MASK	0x2558	SCACHE1_WIN3_MASK
0x2460	SCACHE0_WIN4_MASK	0x2560	SCACHE1_WIN4_MASK
0x2468	SCACHE0_WIN5_MASK	0x2568	SCACHE1_WIN5_MASK
0x2470	SCACHE0_WIN6_MASK	0x2570	SCACHE1_WIN6_MASK
0x2478	SCACHE0_WIN7_MASK	0x2578	SCACHE1_WIN7_MASK
0x2480	SCACHE0_WIN0_MMAP	0x2580	SCACHE1_WIN0_MMAP
0x2488	SCACHE0_WIN1_MMAP	0x2588	SCACHE1_WIN1_MMAP
0x2490	SCACHE0_WIN2_MMAP	0x2590	SCACHE1_WIN2_MMAP
0x2498	SCACHE0_WIN3_MMAP	0x2598	SCACHE1_WIN3_MMAP
0x24a0	SCACHE0_WIN4_MMAP	0x25a0	SCACHE1_WIN4_MMAP
0x24a8	SCACHE0_WIN5_MMAP	0x25a8	SCACHE1_WIN5_MMAP
0x24b0	SCACHE0_WIN6_MMAP	0x25b0	SCACHE1_WIN6_MMAP

3A6000 ಶ ಶ

-	-	0x2970	IO_L2X_WIN6_MASK
-	-	0x2978	IO_L2X_WIN7_MASK
-	-	0x2980	IO_L2X_WIN0_MMAP
-	-	0x2988	IO_L2X_WIN1_MMAP
-	-	0x2990	IO_L2X_WIN2_MMAP
-	-		

MMAP

3- 8 MMAP

[7]	[6]	[5]	[4]
٥	DDR ~ 0 “ interleave_bit IOCSR[0x0400] ” ث ٥ خي ضر 10	ىشج	ٌّ

٥ Cache خي ضر ٦ ↕ ضي SCache

خي ضر كح Cache خي ضر Cache

ث ٥ : (IN_ADDR & MASK) == BASE

خي ضر : OUT_ADDR = (IN_ADDR & ~MASK) | {MMAP[63:10],10 ’ h0}

كح Ω¯ U CPU 0x00000000 - 0x0fffffff ٧ خي ضر

256M ⌠ DDR 0x00000000 - 0x0fffffff ٧ خي ضر 0x10000000-0x17ffffff

⌠ PCI_MEM 0x18000000-0x19ffffff ⌠ PCI_IO

0x1a000000-0x1affffff ⌠ PCI Type0 0x1b000000-0x1bffffff

⌠ PCI Type1 0x40000000-0x7fffffff ⌠ PCI_MEM

~ كح خي ضر غ

∓ CPU خي ضر 8 خي ضر ٥ ث

عج CPU

7	DVFS_v1	R	1 ' b1	1 ـ v1ً
8	Tsensor	R	1 ' b1	1 كً
9		R	1 ' b1	ً
10		R	1 ' b1	
11	Guest Mode	R	1 ' b0	KVM
12	Freq_scale_16	R	1 ' b0	1 16 №
13	Int Remap	R	1 ' b1	1 L
14	SE enabled	R	1 ' b0	1 SE w

4.3 0x0010

ك ٨ ـ O خي ضر 0x0010

4- 4 ٨ ـ O ك

	O			
63:0	Vendor	R	0x6e6f7367_6e6f6f4c	“ Loongson ”

4.4 0x0020

ك O خي ضر 0x0020

4- 5 O ك

	O			
63:0	ID	R	0x00003030_30364133	“ 3A6000 ”

4.5 0x0180

خي ضر 0x0180

4- 6 w ك

O				
0		RW	1 ' b0	
1		RW	1 ' b0	
3:2		RW	2 ' b0	
4	MC0_disable_confspace	RW	1 ' b0	٦ MC0 DDR
5	MC0_defult_confspace	RW	1 ' b1	ṗ
6		RW	1 ' b1	
7	MC0_resetn	RW	1 ' b1	MC0
8	MC0_clken	RW	1 ' b1	٦ MC0
9	MC1_disable_confspace	RW	1 ' b0	٦ MC1 W N

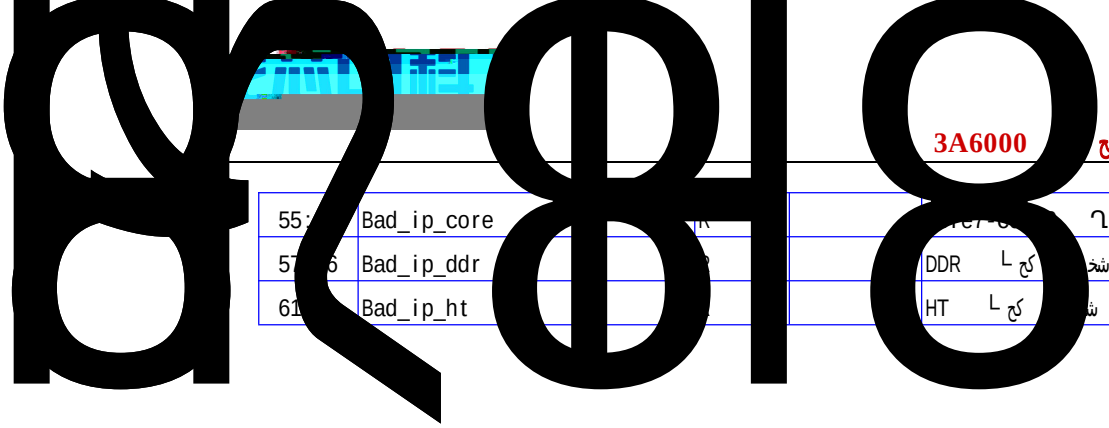
10	MC1_defult_confspace	RW	1 ' b1	ṗ
11		RW	1 ' b1	
12	MC1_resetn	RW	1 ' b1	MC1
13	MC1_clken		1 ' b1	٦ MC1
26:24	HT_freq_scale_ctrl	RW	3 ' b011	HT ك №
27	HT_clken	RW	1 ' b1	٦ HT
30:28				
31				
42:40	Node_freq_ ctrl	RW	3 ' b111	№
43	-	RW	1 ' b1	
63:56	Cpu_version	R	2 ' h3F	CPU

4.6 0x0188

ضي 0x0188

4- 7 ك

	o			
15:0				
19:16	HT sideband	RW	4 ' b0	HT
23:20	I2C	RW	4 ' b0	I2C
27:24	UART	RW	4 ' b0	UART
31:28	SPI	RW	4 ' b1	SPI
35:32	GPIO	RW	4 ' b0	GPIO
39:36	SE UART	RW	4 ' b0	SE UART
43:40	SE SPI	RW	4 ' b0	SE SPI
47:44	SE I2C	RW	4 ' b0	SE I2C
51:48	îϟjŮ	I		



55:	Bad_ip_core		
57 6	Bad_ip_ddr	DDR	
61	Bad_ip_ht	HT	

4.8 8

1) ಶ

6		RW		
6		RW		T 2 N №
		RW		3 ' b000
75:73	L2_FBDLY	RW		3 ' b000
79:76	L2_ICPSEL	RW		4 ' b0111
83:80	L2_FVCO_TUNE_ABS	RW		4 ' b0011
84	L2_SSC_SPRD	RW		0
85	L2_SSC_EN	RW		L2
95:86	-	RW		
115:96	L2_FRAC	RW		L2 №
119:116				
122:120	VDDA_LDO_CTRL	RW		
123	VDDA_LDO_BYPASS	RW		
126:124	VDDD_LDO_CTRL	RW		
127:124	VDDD_LDO_BYPASS	RW		
ï	-	RW		

PLL ouput = clk_r l

NODE NODE_CLOCK_SEL 1
№

[23:14]	MEM_PLL_DIV_LOOPC	RW	0x41	MEM PLL ă
[29:24]	MEM_PLL_DIV_OUT	RW	0x0	MEM PLL ă
[30]	NODE_CLOCK_SEL	RW	0x0	0 MEM_PLL MEM 1 NODE_CLOCK L2 PLL №
[31]	-			
[34:32]	VDDA_LDO_CTRL	RW		
[35]	VDDA_LDO_BYPASS	RW		
[38:36]	VDDD_LDO_CTRL	RW		
[39]	VDDD_LDO_BYPASS	RW		
[40]				

11	core2_en	RW	0x1	2	1
14:12	core3_freqctrl	RW	0x7	3 №	L
15	core3_en	RW	0x1	3	
			:	№ U	/
				№ L +1 /8	

12		RW	0x0	
14	Scahe_1MB	RW	0x0	Scache ⁞ ٧
19:16		RW	0x0	
24		RW	0x0	
31:30	mc_en	RW	0x3	MC L
37:32	interleave_bit	RW	0x0	ṗ ↓ L
39	interleave_en	RW	0x0	ṗ ↓
43:40	ht_control	R		Ht ˜
47:44		RW	0x0	
60:56		RW	0x0	
63:61	Reserved	RW	0x0	

4.13 0x0420

ك L ṗ №w ضي 0x0420

4- 16ʁʍ ì w ⁰ˣʍ ك

	O			
0	disable_jtag	RW	0x0	JTAG o
1	disable_jtag_Core	RW	0x0	JTAG o
2	disable_LA132	RW	0x0	LA132
3	disable_jtag_LA132	RW	0x0	LA132 JTAG o
4	Disable_antifuse0	RW	0x0	fuse
5	Disable_antifuse1	RW	0x0	fuse
6	Disable_ID	RW	0x0	ID
7				
8	resetn_LA132	RW	0x0	LA132 L
9	sleepn 7			

3A

	o			
63:0	sram_ctrl	RW	0x0	ڤ Sram ك

4.16 FUSE0 0x0460

ك № ˜ Fuse0 خي ضر 0x0460

4- 19 FUSE ك

	o			
127:0	Fuse_0	RW	0x0	

4.17 FUSE1 0x0470

ك № ˜ Fuse1 خي ضر 0x0470

4- 20 FUSE ك

	o			
127:0	Fuse_1	RW	0x0	

5

3A6000 ا ǎ SYS_CLOCK ٮ

SYS_CLOCK №≠

3A6000 ك ï HT ك ï LA132 №≠ №

ٮ ك ضي 0x1fe00000 ك

IOCSR ضي ٮ ṗ ضي ك

ضي ضي [17:16] ٧ ṗ

5.1

ǎ SYS_CLOCK 100MHz 25MHz

CHIP_CONFIG[4]

HT PHY ǎ SYS CLOCK PHY 200MHz № ǎ

CHIP_CONFIG[8] SYS CLOCK ǎ 25MHz

HT PHY ض 3.2GHz

3A6000 ï ì

5- 1 ك ṗ

		№	ٮ
Boot Clock	SYS_CLOCK	*1	SPI UART I2C AVS ك
	SYS PLL		SYS PLL ₮
Main Clock	Back PLL	PLL	Node Clock Core Clock HTcore Clock LA132 Clock Mem Clock Stable Clock
Node Clock	Main Clock	*1	HT ك
Core0 Clock	Main Clock	*1	Core0
Core1 Clock	Main Clock	*1	Core1
Core2 Clock	Main Clock	*1	Core2
Core3 Clock	Main Clock	*1	Core3
HTcore Clock	Node Clock	*1	HT ك №

n Clock	MEM PLL	PLL			
	Back PLL	/2 /4 /8			

.2

5- 3 ï w ك

	o			
35:32	freqscale_mode_core	RW	0x0	0: (n+1)/8 1: 1/(n+1)

5.2.2

خي ضر 3A6000 ك №

ك

№ ك L ﾉ ك № ك L

ٯ “ ï w ك ”

L ك خي ضر 0x1fe00000 ˆ ك IOCSR

خي ضر 0x0420

5- 4 ï w ك

	o			
22	freqscale_percore	RW	0x0	ك
23	clken_percore	RW	0x0	

freqscale_percore 1 № ك freqscale

№ ´ freqscale_mode clken_percore 1

№ ك clken L

3A6000 4 8 0 2 4 6 4

L 1 3 5 7 ك 4 5 6

7 ك 0x1fe10000 خي ˜ ك

ك خي ضر 0x1050

5- 5 ك № ك

	o			
4	freqscale_mode	RW	0x0	╠ ك № 0: (n+1)/8 1: 1/(n+1)
3	clken	RW	0x0	╠ ك
2:0	freqscale	RW	0x0	╠ ك №

5.3

clken

5.3.1

IOCSR 0x1fe00000

0x0180

5- 6

42:40	Node0_freq_ctrl	RW	3'b111	0

“1/ +1 ” “ +1 /8 ”

IOCSR 0x1fe00000

0x0420

5- 7

36	freqscale_mode_node	RW	0x0	0: (n+1)/8 1: 1/(n+1)

5.3.2

1212.3

5.4 HT

HT └ك № └ ٪ w ك ٪

خي ضر 0x1fe00000 ˜ ك IOCSR خي ضر 0x0180

5- 8 w ك

	o			
26:24	HT_freq_scale_ctrl	RW	3 ' b111	HT └ك №
27	HT_clken	RW	1 ' b1 ٦ HT

٪ № └ HT └ك ˜ ك № U & ⅲ

GPIO_FUNC_en[13] 1 stable counter ٱ ⌠ GPIO[13] ⌊

GPIO ₹ كح خي ضر 0x1fe00000 ˜ كح IOCSR

خي ضر 0x0500

5- 11 GPIO ₹ كح

	O	0

7 GPIO

3A6000 20 GPIO №ì w

كح ˆ GPIO w ˆ ì

ˆ كح خي ضر 0x1fe00000

7.1 0x0500

خي ضر 0x1fe00000 خي ضر 0x0500

7- 1 ₹ كح

	o			
31:0	GPIO_OEn	RW	32 'hffffffff	GPIO ₹
63:32	GPIO_FUNC_En	RW	32 'hffff0000	GPIO w

7.2 0x0508

خي ضر 0x1fe00000 خي ضر 0x0508

7- 2 ₹ كح

o

7.4 GPIO

7.5 GPIO

3A6000 GPIO ~

GPI000 GPI008 GPI016 " L ك 0~

GPI001 GPI009 GPI017 " L ك 1~

GPI002 GPI010 GPI018 " L ك 2~

GPI003 GPI011 GPI019 " L ك 3~

GPI004 GPI012 " L ك 4~

GPI005 GPI013 " L ك 5~

GPI006 GPI014 " L ك 6~

GPI007 GPI015 " L ك 7~

GPI020-GPI031

GPIO ك GPIO_INT_en L GPIO_INT_POL L

ك

خي ضر 0x1fe00000 خي ضر 0x0510

7- 5 L ك

	O			
31:0	GPIO_INT_Pol	RW	32 ' h0	GPIO 0 - 1 -
63:32	GPIO_INT_en	RW	32 ' h0	GPIO L

L ك ٧ ì GPIO ~ Ü نه

ضي POL 0 1 ٨ Ü ضي L ك

LA32 ↑ O ₈ LA32 bit0 LA32

0 ⅈ bitAA:BB

AA ⌠ BB (AA-BB+1)

₹ 3A6000 w ↓ U ↓ “ˆ ŭ ”

؏ ˆ ₹ ₔ 3A6000 ؏ ₹ ί ₹

₹ ‰ ₹ U

∞ U ↓ ṗ 3A6000 w

8- 1 w ↓

؏ˆ		O		ˆ ŭ
0x0	31:0	PRId	؏	32 ’ h14_d001
0x1	1:0	ARCH	2'b00 LA32 2'b01 LA32 2'b10 LA64 2'b11	2 ’ b10
	2	PGMMU	1 MMU	1 ’ b1
	3	IOCSR	1 IOCSR	1 ’ b1
	11:4	PALEN	خيضر PALEN ⁞ 1	8 ’ d47
	19:12	VALEN	خيضر VALEN ⁞ 1	8 ’ d47
	20	UAL	1	1 ’ b1
	21	RI	1 “ ”	1 ’ b1
	22	EP	1 “ ”	1 ’ b1
	23	RPLV	1 RPLV	1 ’ b1
	24	HP	1 huge page	1 ’ b1
	25	CRC32	1 CRC32 ٧	1 ’ b1
	26	MSG_INT	1	1 ’ b1
0x2	0	FP	1	1 ’ b1
	1	FP_SP	1 ١	1 ’ b1
	2	FP_DP	1 ĭ	1 ’ b1
	5:3	FP_ver	‰ ˆ 1 Δ ˆ ˋl IEEE 754-2008 ‰	3 ’ h1
	6	LSX	1 128 h	1 ’ b1
	7	LASX	1 256 h	1 ’ b1
	14	LLFTP	1 ؏ غ ؏	1 ’ b1

	17:15	LLFTP_ver		كج غ كج ً 1 Δ	3 ' h1
	21	LSPW	1	٨	1 ' b1
	22	LAM	1	AM* ٨	1 ' b1
	0	CCDMA	1	Cache Coherent DMA	1 ' b1
	1	SFB	1	Store Fill Buffer SFB	1 ' b1
	3	LLEXC	1	LL ٌّ \lشجw	1 ' b1
	4	SCDLY	1	SC U w	1 ' b1
	5	LLDBAR	1	LL ـ dbar w	1 ' b1
0x3	6	ITLBHMC	1	ITLB TLB	1 ' b1
	7	ICHMC	1	كج ضْ ICache DCache	1 ' b1
	10:8	SPW_LVL	page walk		3 ' h4
	11	SPW_HP_HF	1	page walk ضي ⌡ ٧ TLB	1 ' b1
	12	RVA	1	w مخ ضر جي	1 ' b1
	16:13	RVMAX-1	ً	ضر جي -1	4 ' h7
0x4	31:0	CC_FREQ		كج غ كج ٧ Hz	N/A
0x5	15:0	CC_MUL	غج	كج غ كج	N/A
	31:16	CC_DIV		كج غ كج №	N/A
	0	PMP	1	كج	1 ' b1
0x6	3:1	PMVER		كج ً 1 Δ	3 ' h1
	7:4	PMNUM		كج -1	4 ' h3
	13:8	PMBITS		كج -1	6 ' h3f
	14	UPM	1	ٌّ كج	1 ' b1
0x10	0	L1 IU_Present	1	ضي Cache Cache	1 ' b1
	1	L1 IU Unify	1	L1 IU_Present Cache Cache	1 ' b0
	2	L1 D Present	1	ضي Cache	1 ' b1
	3	L2 IU Present	1	ضي Cache Cache	1 ' b1
	4	L2 IU Unify	1	L2 IU_Present Cache Cache	1
	5	L2 IU Private	1	L2 IU_Present Cache	1
	6	L2 IU Inclusive	1	L2 IU_Present Cache	1

L1 ´ ج

7	L2 D Present	1	ض	Cache	1 ' b0
8	L2 D Private	1		Cache	i

8.2 3A6000

3A6000 كح IOCSR خي

IOCSR كح ṕ غ JTAG ŋ

IOCSR IOCSRRD.B/H/W/D غ IOCSRWR.B/H/W/D Ώ ὶ

IOCSRRD.B/H/W/D IOCSRRD.B/H/W/D rd, rj ὶ rj كح

IOCSR خي ضر IOCSR عج ṕ Ώ ⌠ rd كح IOCSRWR.B/H/W/D

IOCSRWR.B/H/W/D rd, rjW/ ὶ rj كح IOCSR خي ضر

ضي " rdÏ كح Ώ IOCSR IOCSRRD.B/H/W/D غ jd, Ð7

ضي

IOCSRRD.B/HW/ D غ jd, Ð ˜ ⁄ خي ضر

9 Cache SCache

SCache 3A6

Slock2_mask	0x0250	[47:0]	2	o
Slock3_valid	0x0218	[63:63]	3	o
Slock3_addr	0x0218			

	en			
36	MCC clean shared replace en	RW	1 ' b0	

10

3A6000 ك 8 ك IPI BIOS Ω

ـ غ ض ك غ

3A6000 □ خي ض ٣

ك ك U №≠

10.1

3A6000 ↓ كـ خي ض 0x1fe00000 ـ

ك IOCSR خي ض 0x3ff00000 ـ ك

disable_0x3ff0 L ـ ٬ ك غ خي ض 10- 1 ⌠ 10- 5

3A6000 ´ 8 ـ ض 3

ـ ↕ 8 ⅞№ خي ض ␣ ṗ

خي ض خي ض ض [17:16] ₰ ṗ ـ 4 7 خي ض 0x1fe10000

٬ ك خي 0 3

10- 1 ك ـ ك ĭ ì w

O	Ω							
IPI_Status	R	32	ك	1	'	ك	INT4	
IPI_Enable	RW	32	ك	L	٦			
IPI_Set	W	32	ك	Ω 1	↕	STATUS	ك	1
IPI_Clear	W	32	ك	Ω 1	↕	STATUS	ك	0
MailBox0	RW		ك	Ω	ă	64	32	uncache
MailBox01	RW		ك	Ω	ă	64	32	uncache
MailBox02	RW		ك	Ω	ă	64	32	uncache
MailBox03	RW		ك	Ω	ă	64	32	uncache

ض 3A6000 ك ـ ك ĭ ì w

10- 2 0ـ ك ك ↓

O	خي ض					
Core0_IPI_Status	0x1000	R	0ـ	ك	IPI_Status	ك
Core0_IPI_Enalbe	0x1004	RW	0ـ	ك	IPI_Enalbe	ك

Core0_IPI_Set	0x1008	W	0ﺵ ﻙ	IPI_Set ﻙ
Core0_IPI_Clear	0x100c	W	0ﺵ ﻙ	IPI_Clear ﻙ
Core0_MailBox0	0x1020	RW	0ﺵ ﻙ	IPI_MailBox0 ﻙ
Core0_ MailBox1	0x1028	RW	0ﺵ ﻙ	IPI_MailBox1 ﻙ
Core0_ MailBox2	0x1030	RW	0ﺵ ﻙ	IPI_MailBox2 ﻙ
Core0_ MailBox3	0x1038	RW	0ﺵ ﻙ	IPI_MailBox3 ﻙ

10- 3 1ﺵ ﻙ ﻙ ↓

O	خﻲﺿ		
Core1_IPI_Status	0x1100	R	1ﺵ ﻙ IPI_Status ﻙ
Core1_IPI_Enalbe	0x1104	RW	1ﺵ ﻙ IPI_Enalbe ﻙ
Core1_IPI_Set	0x1108	W	1ﺵ ﻙ IPI_Set ﻙ
Core1_IPI_Clear	0x110c	W	1ﺵ ﻙ IPI_Clear ﻙ
Core1_MailBox0	0x1120	R	1ﺵ ﻙ IPI_MailBox0 ﻙ
Core1_ MailBox1	0x1128	RW	1ﺵ ﻙ IPI_MailBox1 ﻙ
Core1_ MailBox2	0x1130	W	1ﺵ ﻙ IPI_MailBox2 ﻙ
Core1_ MailBox3	0x1138	W	1ﺵ ﻙ IPI_MailBox3 ﻙ

10- 4 2ﺵ ﻙ ﻙ ↓

O	خﻲﺿ		
Core2_IPI_Status	0x1200	R	2ﺵ ﻙ IPI_Status ﻙ
Core2_IPI_Enalbe	0x1204	RW	2ﺵ ﻙ IPI_Enalbe ﻙ
Core2_IPI_Set	0x1208	W	2ﺵ ﻙ IPI_Set ﻙ
Core2_IPI_Clear	0x120c	W	2ﺵ ﻙ IPI_Clear ﻙ
Core2_MailBox0	0x1220	R	2ﺵ ﻙ IPI_MailBox0 ﻙ
Core2_ MailBox1	0x1228	RW	2ﺵ ﻙ IPI_MailBox1 ﻙ
Core2_ MailBox2	0x1230	W	2ﺵ ﻙ IPI_MailBox2 ﻙ
Core2_ MailBox3	0x1238	W	2ﺵ ﻙ IPI_MailBox3 ﻙ

10- 5 3ﺵ ﻙ ﻙ ↓

O	خﻲﺿ		
Core3_IPI_Status	0x1300	R	3ﺵ ﻙ IPI_Status ﻙ
Core3_IPI_Enalbe	0x1304	RW	3ﺵ ﻙ IPI_Enalbe ﻙ
Core3_IPI_Set	0x1308	W	3ﺵ ﻙ IPI_Set ﻙ
Core3_IPI_Clear	0x130c	W	3ﺵ ﻙ IPI_Clear ﻙ
Core3_MailBox0	0x1320	R	3ﺵ ﻙ IPI_MailBox0 ﻙ
Core3_ MailBox1	0x1328	RW	3ﺵ ﻙ IPI_MailBox1 ﻙ
Core3_ MailBox2	0x1330	W	3ﺵ ﻙ IPI_MailBox2 ﻙ
Core3_ MailBox3	0x1338	W	3ﺵ ﻙ IPI_MailBox3 ﻙ

↓ ₹ 3A6000 ﻙ 0 3

ﺵ ﻙ ↓ 3A6000 ´ 8 ﺵ

0x1fe10000

10.2

3A6000

10- 6

O		sL€			
perCore_IPI_Status	0x1000	R		IPI_Status	
perCore_IPI_Enalbe	0x1004	RW		IPI_Enalbe	
perCore_IPI_Set	0x1008	W		IPI_Set	
perCore_IPI_Clear	0x100c	W		IPI_Clear	
perCore_MailBox0	0x1020	RW		IPI_MailBox0	
perCore_ MailBox1	0x1028	RW		IPI_MailBox1	
perCore_ MailBox2	0x1030	RW		IPI_MailBox2	
perCore_ MailBox3	0x1038	RW		IPI_MailBox3	

h MailBox

			0 - MailBox0 32 1 - MailBox0 32 2 - MailBox1 32 3 - MailBox1 32 4 - MailBox2 32 5 - MailBox2 32 6 - MailBox3 32 7 - MailBox4 32 [1:0]
FREQ_Send	0x1058	WO	32 كج [31] 1 [30:27] ٬Ω mask 32 ٬Ω ٬Ω خي ضر 1000b ٬Ω 0-2 0000b ↕ 0-3 ٬Ω [26] [25:16] كج ˜ [15:5] [4:0] ٬Ω كج كج IOCSR[0x1050]

Mail_Send كج ₇ ˜ ΰ 32 ΰ 64

№ ΰ غج ضي Mail_Box ṗ ì

ΰ Mail_Box U ΰ

10.3

كج ∧ ↕ ضي ضي

خي ضر كج كج₇ ٬Ω

₹ ╠ ⌠ IPI_Send Mail Send Freq Send Any Send كج˜

خي ضر ì

10- 8 كج كج

O	خي ضر		
ANY_Send	0x1158	WO	64 كج كج [63:32] ٬Ω [31] 1 [30:27] ٬Ω mask 32 ٬Ω ٬Ω خي ضر 1000b ٬Ω 0-2 0000b ↕ 0-3 ٬Ω [26]

			[25:16] كج ٍّ [15:0] ٰΩ كج خفيض

11 I/O

3A6000 □ I0

HT └ר ¯ № ŭ w № ≠

3A6000 ṗ └ר ˜ └ר

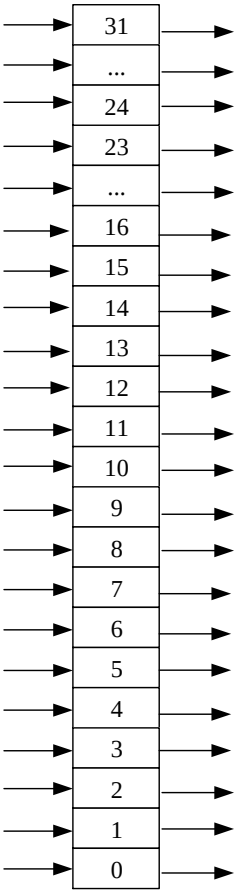
№ ≠ └ר ר ╠ ר

11.1 I/O

3A6000 32 ⁻

I0 ˜ ʔ ŭ ĭ ר

№ ŭ ₇ □ ר ṗ ר



IP0
IP1
IP2
IP3

Enable ლ Intenset Intenclr ჯ Inten Intenset
Intenset ლ Ⴊ 1 Intenclr
Intenclr ლ Ⴊ 1 Inten ლ ṻ ╠ Ⴣ ,
ṻ ˜ Intedge ლ Ⴊ 1 ṻ Ⴊ 0
ṻ ˜ Intenclr □

11- 1 L ლ

/					
	Intedge	Inten	Intenset	Intenclr	
0	RW / 0	R / 0	RW / 0	RW / 0	GPIO24/16/8/0/SC0
1	RW / 0	R / 0	RW / 0	RW / 0	GPIO25/17/9/1/SC1
2	RW / 0	R / 0	RW / 0	RW / 0	GPIO26/18/10/2/SC2
3	RW / 0	R / 0	RW / 0	RW / 0	GPIO27/19/11/3/SC3
4	RW / 0	R / 0	RW / 0	RW / 0	GPIO28/20/12/4
5	RW / 0	R / 0	RW / 0	RW / 0	GPIO29/21/13/5
6	RW / 0	R / 0	RW / 0	RW / 0	GPIO30/22/14/6
7	RW / 0	R / 0	RW / 0	RW / 0	GPIO31/23/15/7
8	RW / 0	R / 0	RW / 0		

11.1.1

3A3000 كج ٰl خي ضر ̃ 0x1fe00000 ̃

كج IOCSR 0x3ff00000 خي ضر ̃

كج disable_0x3ff0 L 3A6000 ´ 8

̃ ضي 3̃ ↕ 8 ⅞№

خي ضر ٰ̀ ṕ خي ضر خي ضر ضي خي ضر [17:16] ₰ ṕ ̃

4 7 خي ضر 0x1fe10000 ĺ كج خي 0 3

11- 2 IO L خي ضر كج

O	خي ضر		
Intisr	0x1420	32	كج
Inten	0x1424	32	كج
Intenset	0x1428	32	كج
Intenclr	0x142c	32	كج
Intedge	0x1434	32	Ũ كج
CORE0_INTISR	0x1440	CORE0	32
CORE1_INTISR	0x1448	CORE1	32
CORE2_INTISR	0x1450	CORE2	32
CORE3_INTISR	0x1458	CORE	

11- 4 خي ضر كج

O	خي ضر		O	خي ضر	
Entry0	0x1400	GPIO24/16/8/0	Entry16	0x1410	
Entry1	0x1401	GPIO25/17/9/1	Entry17	0x1411	
Entry2	0x1402	GPIO26/18/10/2	Entry18	0x1412	
Entry3	0x1403	GPIO27/19/11/3	Entry19	0x1413	
Entry4	0x1404	GPIO28/20/12/4	Entry20	0x1414	
Entry5	0x1405	GPIO29/21/13/5	Entry21	0x1415	
Entry6	0x1406	GPIO30/22/14/6	Entry22	0x1416	
Entry7	0x1407	GPIO31/23/15/7	Entry23	0x1417	
Entry8	0x1408	I2C0	Entry24	0x1418	HT1-int0
Entry9	0x1409	I2C1	Entry25	0x1419	HT1-int1
Entry10	0x140a	UART0	Entry26	0x141a	HT1-int2
Entry11	0x140b	MC0	Entry27	0x141b	HT1-int3
Entry12	0x140c	MC1/AVS	Entry28	0x141c	HT1-int4
Entry13	0x140d	SPI	Entry29	0x141d	HT1-int5
Entry14	0x140e	Thsens	Entry30	0x141e	HT1-int6
Entry15	0x140f	UART1	Entry31	0x141f	HT1-int7

11.1.2

ضي 3A6000 □ ˜ كج

كج خي ضر خي ضر □

□ ╠ كج

11- 5 كج كج

O	خي ضر	
perCore_INTISR	0x1010	╠ كج 32

11.2 I/O

`I ∕ IO 3A6000 I/O HT

256 №Ŭ Ɏ كج ٬P HT Ŭ ٬I IO

كح ” كح w ‘ ì ╠ IO ضي ṗ

0x0420 خي ضر IOCSR كح ˆ 0x1fe00000 خي ضر

11- 6 ì w كح

	O			
48	EXT_INT_en	RW	0x0	IO

╠ № ü ï ü HT ˆ ضي IO

h 256 ˆ

11.2.1

ˆ خي ضر كح ì كح IO ˆ

3A6000 ´ كح كح ˆ 0x1fe00000

8 ↕ 8 3ˆ ضي ˆ

[17:16] خي ضر خي ضر ṗ ¼ خي ضر ⅞№ 8

كح ì 0x1fe10000 خي ضر 4 7 ˆ ṗ ₰

خي 0 3

11- 7 IO كح

O	خي ضر			
EXT_IOIen[63:0]	0x1600		IO	[63:0]
EXT_IOIen[127:64]	0x1608		IO	[127:64]
EXT_IOIen[191:128]				

11- 10 ۸ ž

EXT_IOImap3	0x14C3	EXT_IOI[127:96]
EXT_IOImap4	0x14C4	EXT_IOI[159:128]
EXT_IOImap5	0x14C5	EXT_IOI[191:160]
EXT_IOImap6	0x14C6	EXT_IOI[223:192]
EXT_IOImap7	0x14C7	EXT_IOI[255:224]

ع 11- 13 خي ضر غ أ كح L 8 ع

h كح h 11- 15 ضي [7:4] ï 11- 14

3ً كح EXT_IOI_node_type4 ⌠ 0x48

كح كح 11- 13

3:0	h كح ً
7:4	11- 15

U ً كح ضي EXT_IOIbounce ً EXT_IOIbounce 1 ضي ً № Ü

0x0013 № Ü ضي 0 0 0 1 0 2 EXT_IOI_node_type2 0x27 11- 15 11- 13

1 0 1 1 1 2 4 0 4 1 4 2

ٿھ № Ü EXT_IOIbounce 0 ً bitmap ٧

1 0 ضر Ü

كح كح خي ضر 11- 14

O	خي ضر	
EXT_IOImap_Core0	0x1C00	EXT_IOI[0] كح
EXT_IOImap_Core1	0x1C01	EXT_IOI[1] كح
EXT_IOImap_Core2	0x1C02	EXT_IOI[2] كح
ا٠ ا٠		
EXT_IOImap_Core254	0x1CFE	EXT_IOI[254] كح
EXT_IOImap_Core255	0x1CFF	EXT_IOI[255] كح

11- 15

O	خي ضر		
EXT_IOI_node_type0	0x14A0	16	h قمم 0
EXT_IOI_node_type1	0x14A2	16	h قمم 1
EXT_IOI_node_type2	0x14A4	16	h قمم 2

ا٠ ا٠		
EXT_IOI_node_type15	0x14BE	16 h 15 قسم

11.2.2

ك ك ض ك

ك ٧ h خي ض ŭ ∓ ˜ ⌠ ╣

11- 16 ╣ ك IO ك

O	خي ض		
perCore_EXT_IOIsr[63:0]	0x1800	╣ ك IO	[63:0]
perCore_EXT_IOIsr[127:64]	0x1808	╣ ك IO	[127:64]
perCore_EXT_IOIsr[191:128]	0x1810	╣ ك IO	[191:128]
perCore_EXT_IOIsr[255:192]	0x1818	╣ ك IO	[255:192]

11.2.3 IO

IO ـ № ŭ ض ك ٧ IO ŭ

ك IO ˜ ≠ ك

ك

11- 17 IO ŭ ك

O	خي ض		
EXT_IOI_send	0x1140	WO	IO ك [7:0] h

11.2.4 IO HT

HT HT HT ك ṗ ⌡ HT

ك 256 h 'P 256 h № 4 8 'P ٤

⌠ ك HT IO

٧ ٤ ٣ ṗ № ŭ ٧ 4

8 ٤ № ŭ

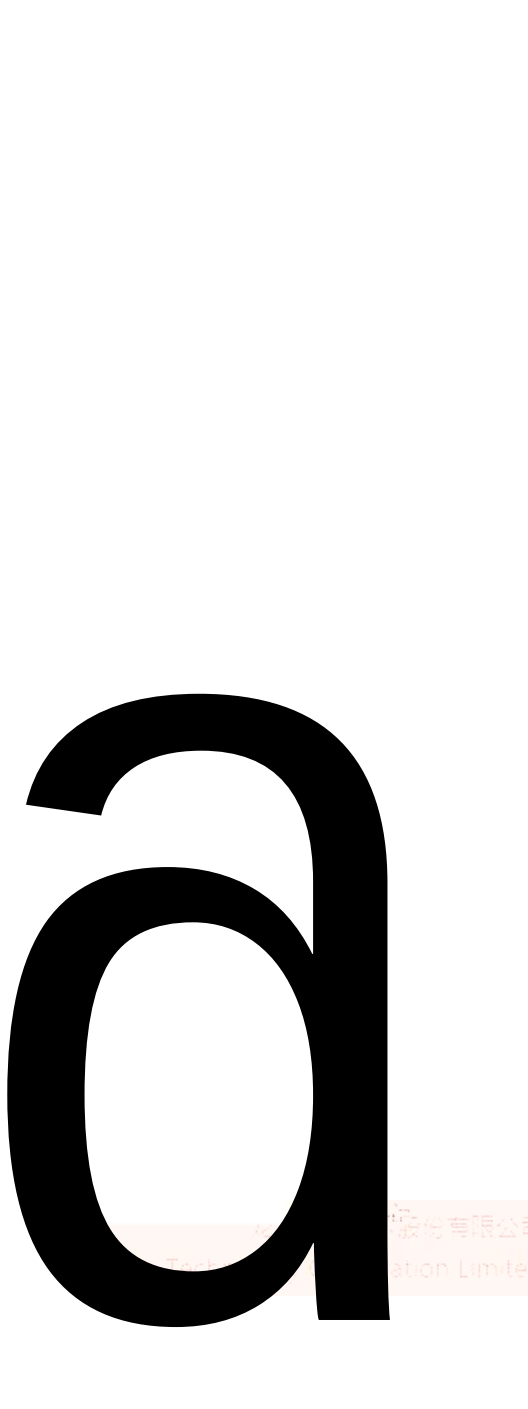
IO HT HT ك ŭ ك

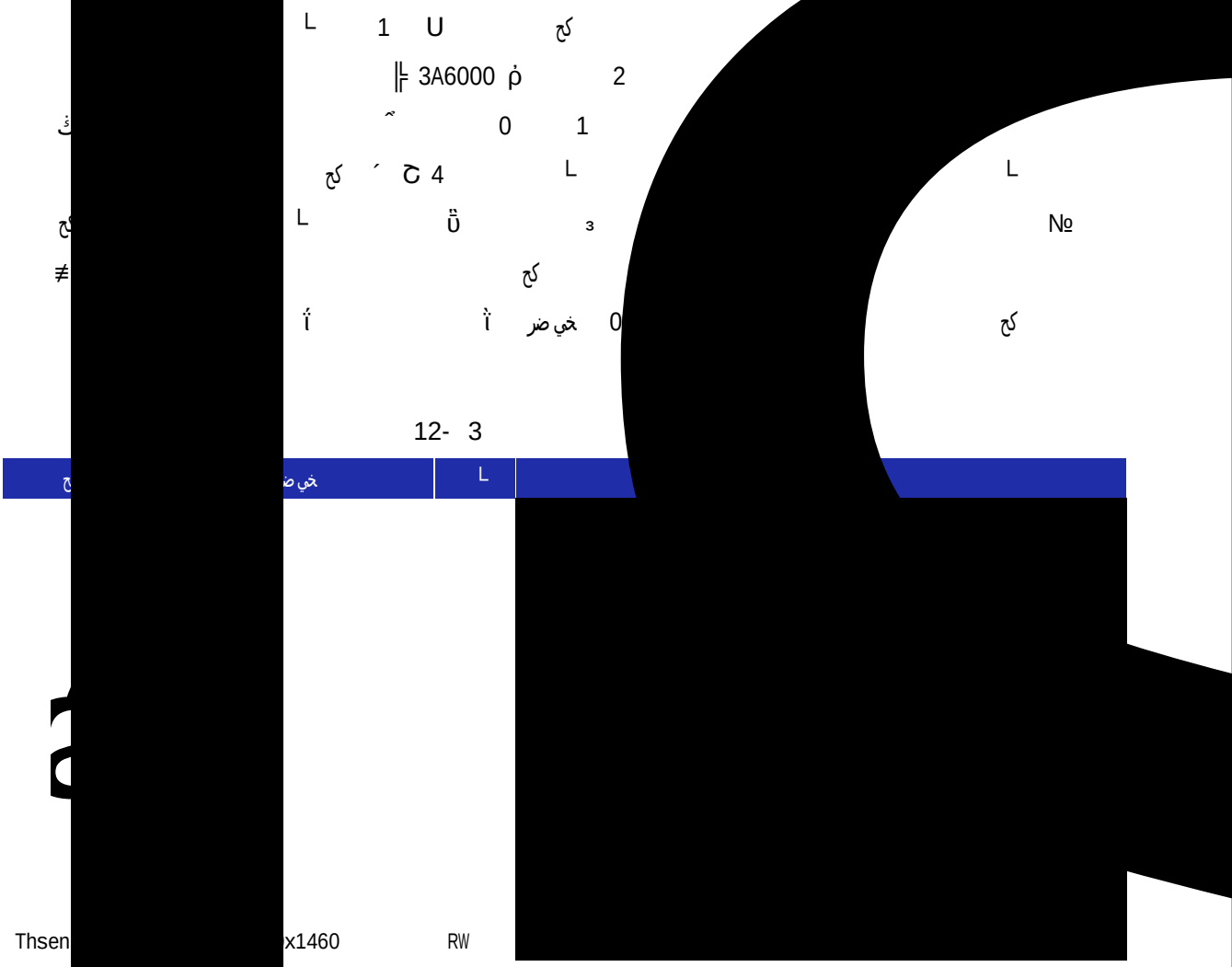
12

12.1

g

3A6000 ρ 0x1fe00198 g





Thsen x1460 RW

[ ]	Scale_ e0	0	
[8:	Scal 0	0	
[11:10]	Scale_Sel0	0	ע
[14:12]	Scale_freq0	№	
[23:16]	Scale_gate1	1	
[24:24]	Scale_en1	1	
[27:26]	Scale_Sel1	1	ע
[30:28]	Scale_freq1	№	
[39:32]	Scale_gate2	2	
[40:40]	Scale_en2	2	
[43:42]	Scale_Sel2	2	ע
[46:44]	Scale_freq2	№	
[55:48]			

L ע

Thsens_freq_scale	0x1480	RW

PROCHOTn PROCH L ˆ Ŭ

THERMTRIPn L Ŭ

Ĭ L

12- 5 L

	0x1498	RW	[0:0] prochotn_oe PROCHOTn 1 [5:4] prochotn_o_sel PROCHOTn [10:8] prochotn_freq_scale PROCHOTn [17:16] thermtripn_o_sel THERMTRIPn

12.5

3A6000 2 / 1

0x1FE00000 IOCSR

0x01580+vtsensor_id<<4, 0x01588+vtsensor_id<<4

11:9	Temp_cluster	RW	0	ん Thsens_trigger

12- 7 ん ん

	O			
3	Out_mode	R	0	ん 0 1 ｲ
6:4	Out_cluster	R	0	ん
7	Overflow	R	0	ん
29:16	Data	R	0	ん

=data*820/0x4000 - 311 -40 ~ 125

ｲ=(data+110)*1.226/0x1000

13 DDR4 SDRAM

3A6000 كج ṗ ṗ └كج DDR4 SDRAM ‰ JESD79-4

13.1 DDR4 SDRAM

3A6000 كج 4 CS ¨ Ƈ 22 خي ضر ٧ 18 ↓ ضر
خي 2 Bank غ 2 Bank Group ĩ ↓ خي ضر RASn CASn
غ Wen

3A6000 كج ضي كج ĩ ṗ فهم ˜ DDR4 └كج ă̈
ĩ CS_n 4 خي ضر ROW 18 ↓ خي ضر COL
12 BANK 2 DDR4 BANK Group 2
CPU ŭ ṗ ˜خي ضر └كج ṗ خي ضر

3A6000 كج ṗ └ ₇ ĩ كج ṗ /
Ω ضي ṗ /Ω ṗ └ Slave State
3A6000 كج ṗ └كج ĩ
ο ث Ω
ṗ ث ▫▫
كج Ω ο ˜ ṗ ă̈
ECC 1 غ 2 1 ـ
DDR4 SDRAM ă̈ x8 x16 x4
└كج PHY 1/2
مخ 800Mbps-3200Mbps

13.2 DDR4 SDRAM

13.2.1

13- 1 ṗ └كج ˜ ă̈ ↓

Offset	63:56	55:48	47:40	39:32	31:24	23:16	15:8	7:0
PHY								

Offset	63:56	55:48	47:40	39:32	31:24	23:16	15:8	7:0
0x0000	`						version(RD)	
0x0008		switch_byte48	x4_mode	ddr3_mode			capability RD	
0x0010							dram_init(RD)	init_start
0x0018								
							preamble2	rdfifo_valid
0x0028		rdfifo_empty(RD)				Overflow(RD)		
0x0030`		dll_value(RD)	dll_init_done(RD)	dll_lock_mode	dll_bypass	dll_adjj_cnt	dll_increment	dll_start_point
0x0038				dll_dbl_fix			dll_close_disabl e	dll_ck
0x0040								
0x0048							clken_ckca	
0x0050								
0x0058							clken_ds_0	
0x0060								
0x0068							clken_ds_1	
0x0070								
0x0078								

Offset	63:56	55:48	47:40	39:32	31:24	23:16	15:8	7:0
0x0110	rdodt_ctrl_0	rdgate_len_0	rdgate_mode_0	rdgate_ctrl_0			dqs_oe_ctrl_0	dq_oe_ctrl_0
0x0118				odt_len_add_0		dly_2x_0	redge_sel_0	rdddqs_phase_0(RD)
0x0120	w_bdly0_0[31:28]	w_bdly0_0[27:24]	w_bdly0_0[23:20]	w_bdly0_0[19:16]	w_bdly0_0[15:12]	w_bdly0_0[11:8]	w_bdly0_0[7:4]	w_bdly0_0[3:0]
0x0128		w_bdly0_0[59:56]	w_bdly0_0[55:52]	w_bdly0_0[51:48]	w_bdly0_0[47:44]	w_bdly0_0[43:40]	w_bdly0_0[39:36]	w_bdly0_0[35:32]
0x0130	w_bdly1_0[24:21]	w_bdly1_0[20:18]	w_bdly1_0[17:15]	w_bdly1_0[14:12]	w_bdly1_0[11:9]	w_bdly1_0[8:6]	w_bdly1_0[5:3]	w_bdly1_0[2:0]
0x0138								w_bdly1_0[27:26]
0x0140							rg_bdly_0[7:4]	rg_bdly_0[3:0]
0x0148								
0x0150	rdqsp_bdly_0[31:28]	rdqsp_bdly_0[27:24]	rdqsp_bdly_0[23:20]	rdqsp_bdly_0[19:16]	rdqsp_bdly_0[15:12]	rdqsp_bdly_0[11:8]	rdqsp_bdly_0[7:4]	rdqsp_bdly_0[3:0]
0x0158								rdqsp_bdly_0[35:32]
0x0160	rdqsn_bdly_0[31:28]	rdqsn_bdly_0[27:24]	rdqsn_bdly_0[23:20]	rdqsn_bdly_0[19:16]	rdqsn_bdly_0[15:12]	rdqsn_bdly_0[11:8]	rdqsn_bdly_0[7:4]	rdqsn_bdly_0[3:0]
0x0168								rdqsn_bdly_0[35:32]
0x0170	rdq_bdly_0[24:21]	rdq_bdly_0[20:18]	rdq_bdly_0[17:15]	rdq_bdly_0[14:12]	rdq_bdly_0[11:9]	rdq_bdly_0[8:6]	rdq_bdly_0[5:3]	rdq_bdly_0[2:0]
0x0178								rdq_bdly_0[27:26]
0x0180					dll_1xdly_1	dll_1xgen_1	dll_wrdqs_1	dll_wrdq_1
0x0188		vref_sample_1	vref_clk_inv_1	dll_vref_1	vref_dly_1	dll_gate_1	dll_rddqs1_1	dll_rddqs0_1
0x0190	rdodt_ctrl_1	rdgate_len_1	rdgate_mode_1	rdgate_ctrl_1			dqs_oe_ctrl_1	dq_oe_ctrl_1
0x0198				odt_len_add_1		dly_2x_1	redge_sel_1	rdddqs_phase_1(RD)
0x01a0	w_bdly0_1[31:28]	w_bdly0_1[27:24]	w_bdly0_1[23:20]	w_bdly0_1[19:16]	w_bdly0_1[15:12]	w_bdly0_1[11:8]	w_bdly0_1[7:4]	w_bdly0_1[3:0]
0x01a8		w_bdly0_1[59:56]	w_bdly0_1[55:52]	w_bdly0_1[51:48]	w_bdly0_1[47:44]	w_bdly0_1[43:40]	w_bdly0_1[39:36]	w_bdly0_1[35:32]
0x01b0	w_bdly1_1[24:21]	w_bdly1_1[20:18]	w_bdly1_1[17:15]	w_bdly1_1[14:12]	w_bdly1_1[11:9]	w_bdly1_1[8:6]	w_bdly1_1[5:3]	w_bdly1_1[2:0]
0x01b8								w_bdly1_1[27:26]
0x01c0							rg_bdly_1[7:4]	rg_bdly_1[3:0]
0x01c8								
0x01d0	rdqsp_bdly_1[31:28]	rdqsp_bdly_1[27:24]	rdqsp_bdly_1[23:20]	rdqsp_bdly_1[19:16]	rdqsp_bdly_1[15:12]	rdqsp_bdly_1[11:8]	rdqsp_bdly_1[7:4]	rdqsp_bdly_1[3:0]
0x01d8								rdqsp_bdly_1[35:32]
0x01e0	rdqsn_bdly_1[31:28]	rdqsn_bdly_1[27:24]	rdqsn_bdly_1[23:20]	rdqsn_bdly_1[19:16]	rdqsn_bdly_1[15:12]	rdqsn_bdly_1[11:8]	rdqsn_bdly_1[7:4]	rdqsn_bdly_1[3:0]
0x01e8								rdqsn_bdly_1[35:32]
0x01f0	rdq_bdly_1[24:21]	rdq_bdly_1[20:18]	rdq_bdly_1[17:15]	rdq_bdly_1[14:12]	rdq_bdly_1[11:9]	rdq_bdly_1[8:6]	rdq_bdly_1[5:3]	rdq_bdly_1[2:0]
0x01f8								rdq_bdly_1[27:26]
0x0200					dll_1xdly_2	dll_1xgen_2	dll_wrdqs_2	dll_wrdq_2
0x0208		vref_sample_2	vref_clk_inv_2	dll_vref_2	vref_dly_2	dll_gate_2	dll_rddqs1_2	dll_rddqs0_2
0x0210	rdodt_ctrl_2	rdgate_len_2	rdgate_mode_2	rdgate_ctrl_2			dqs_oe_ctrl_2	dq_oe_ctrl_2

Offset

Offset	63:56	55:48	47:40	39:32	31:24	23:16	15:8	7:0
0x0428		w_bdly0_6[59:56]	w_bdly0_6[55:52]	w_bdly0_6[51:48]	w_bdly0_6[47:44]	w_bdly0_6[43:40]	w_bdly0_6[39:36]	w_bdly0_6[35:32]
0x0430	w_bdly1_6[24:21]	w_bdly1_6[20:18]	w_bdly1_6[17:15]	w_bdly1_6[14:12]	w_bdly1_6[11:9]	w_bdly1_6[8:6]	w_bdly1_6[5:3]	w_bdly1_6[2:0]
0x0438								w_bdly1_6[27:26]
0x0440							rg_bdly_6[7:4]	rg_bdly_6[3:0]
0x0448								
0x0450	rdqsp_bdly_6[31:28]	rdqsp_bdly_6[27:24]	rdqsp_bdly_6[23:20]	rdqsp_bdly_6[19:16]	rdqsp_bdly_6[15:12]	rdqsp_bdly_6[11:8]	rdqsp_bdly_6[7:4]	rdqsp_bdly_6[3:0]
0x0458								rdqsp_bdly_6[35:32]
0x0460	rdqsn_bdly_6[31:28]	rdqsn_bdly_6[27:24]	rdqsn_bdly_6[23:20]	rdqsn_bdly_6[19:16]	rdqsn_bdly_6[15:12]	rdqsn_bdly_6[11:8]	rdqsn_bdly_6[7:4]	rdqsn_bdly_6[3:0]
0x0468								rdqsn_bdly_6[35:32]
0x0470	rdq_bdly_6[24:21]	rdq_bdly_6[20:18]	rdq_bdly_6[17:15]	rdq_bdly_6[14:12]	rdq_bdly_6[11:9]	rdq_bdly_6[8:6]	rdq_bdly_6[5:3]	rdq_bdly_6[2:0]
0x0478								rdq_bdly_6[27:26]
0x0480					dll_1xdly_7	dll_1xgen_7	dll_wrdqs_7	dll_wrdq_7
0x0488		vref_sample_7	vref_clk_inv_7	dll_vref_7	vref_dly_7	dll_gate_7	dll_rddqs1_7	dll_rddqs0_7
0x0490	rdodt_ctrl_7	rdgate_len_7	rdgate_mode_7	rdgate_ctrl_7			dqs_oe_ctrl_7	dq_oe_ctrl_7
0x0498				odt_len_add_7		dly_2x_7	redge_sel_7	rddqs_phase_7(RD)
0x04a0	w_bdly0_7[31:28]	w_bdly0_7[27:24]	w_bdly0_7[23:20]	w_bdly0_7[19:16]	w_bdly0_7[15:12]	w_bdly0_7[11:8]	w_bdly0_7[7:4]	w_bdly0_7[3:0]
0x04b8								w_bdly1_7[27:26]
0x04c0							rg_bdly_7[7:4]	rg_bdly_7[3:0]
0x04c8								
0x04d0	rdqsp_bdly_7[31:28]	rdqsp_bdly_7[27:24]	rdqsp_bdly_7[23:20]	rdqsp_bdly_7[19:16]	rdqsp_bdly_7[15:12]	rdqsp_bdly_7[11:8]	rdqsp_bdly_7[7:4]	rdqsp_bdly_7[3:0]
0x04d8								rdqsp_bdly_7[35:32]
0x04e0	rdqsn_bdly_7[31:28]	rdqsn_bdly_7[27:24]	rdqsn_bdly_7[23:20]	rdqsn_bdly_7[19:16]	rdqsn_bdly_7[15:12]	rdqsn_bdly_7[11:8]	rdqsn_bdly_7[7:4]	rdqsn_bdly_7[3:0]
0x04e8								rdqsn_bdly_7[35:32]
0x04f0	rdq_bdly_7[24:21]	rdq_bdly_7[20:18]	rdq_bdly_7[17:15]	rdq_bdly_7[14:12]	rdq_bdly_7[11:9]	rdq_bdly_7[8:6]	rdq_bdly_7[5:3]	rdq_bdly_7[2:0]
0x04f8								rdq_bdly_7[27:26]
0x0500					dll_1xdly_8	dll_1xgen_8	dll_wrdqs_8	dll_wrdq_8
0x0508		vref_sample_8	vref_clk_inv_8	dll_vref_8	vref_dly_8	dll_gate_8	dll_rddqs1_8	dll_rddqs0_8
0x0510	rdodt_ctrl_.doate_8e_							

	63:56	55:48	47:40	39:32	31:24	23:16	15:8	7:0
CTL								
0x1000	tMRD	tRP	tWLDQSEN	tMOD	tXPR		tCKE	tRESET
0x1008								tODTL
0x1010	tREFretention				tRFC		tREF	
0x1018	tCKESR	tXSRD	tXS		tRFC_dlr			tREF_IDLE
0x1020								

Offset	63:56	55:48	47:40	39:32	31:24	23:16	15:8	7:-7k4

Offset	63:56	55:48	47:40	39:32	31:24	23:16	15:8	7:0
0x1260	retry_cnt(RD)					rbuffer_max(RD)	rdfifo_depth	stat_en
0x1268	pm_rdage_low		pm_rdage_up		pm_pref_near_full	pm_hot_en	pm_hot_minus	pm_hot_count
0x1270	pm_stb_error(RO)			pm_stb_deb_cnt_sel	pm_stb_dbg_cnt			
0x1278	pm_stb_adjust				pm_stb_distance	stb_context_gnt	pm_stb_cold_time	
0x1280	aw_512_align		rd_before_wr	ecc_enable		int_vector(RD)	int_trigger(RD)	int_enable
0x1288				pm_stb_arprior_cfg				
0x1290						i		

Offset	63:56	55:48	47:40	39:32	31:24	23:16	15:8	7:0
0x13d0	odt_rd_cs_map							

Offset	63:56	55:48	47:40	39:32	31:24	23:16	15:8	7:0
⋮								
0x1580	win0_mask							
0x1588	win1_mask							
0x1590	win2_mask							
0x1598	win3_mask							
0x15a0	win4_mask							
0x15a8	win5_mask							
0x15b0	win6_mask							
0x15b8	win7_mask							
⋮								
0x1600	win0_mmap							
0x1608	win1_mmap							
0x1610	win2_mmap							
0x1618	win3_mmap							
0x1620	win4_mmap							
0x1628	win5_mmap							
0x1630	win6_mmap							
0x1638	win7_mmap							
⋮								
0x1680	write_train_data[63:0]							
0x1688	write_train_data[127:64]							
0x1690	write_train_data[191:128]							
0x1698	write_train_data[255:192]							
0x16a0	write_train_data[319:256]							
0x16a8	write_train_data[383:320]							
0x16b0	write_train_data[447:384]							
0x16b8	write_train_data[511:448]							
0x16c0	write_train_ecc_data[63:0]							
0x16c8		train_write_n	obj_addr		train_ecc_cmd_en		rw_train_req	rw_train_mode
⋮								
0x1700							acc_hp	acc_en
0x1708	acc_fake_b				acc_fake_a			
0x1710								

Offset

Offset	63:56	55:48	47:40	39:32	31:24	23:16	15:8	7:0
0x21a8	cs_turnaround(RO)							
0x21b0	bg_conflict(RO)							
｜｜								
0x2300						sm_leveling		sm_init
0x2308								
0x2310		sm_rank_03		sm_rank_02		sm_rank_01		sm_rank_00
0x2318		sm_rank_07		sm_rank_06		sm_rank_05		sm_rank_04
0x2320		sm_rank_11		sm_rank_10		sm_rank_09		sm_rank_08
0x2328		sm_rank_15		sm_rank_14		sm_rank_13		sm_rank_12
0x2330		sm_rank_19		sm_rank_18		sm_rank_17		sm_rank_16
0x2338		sm_rank_23		sm_rank_22		sm_rank_21		sm_rank_20
0x2340		sm_rank_27		sm_rank_26		sm_rank_25		sm_rank_24
0x2348		sm_rank_31		sm_rank_30		sm_rank_29		sm_rank_28
｜｜								
0x2430	cache_monitor_cnt(RO)							
0x2438					cache_monitor_cnt(RO)			

Offset	63:56	55:48	47:40	39:32	31:24	23:16	15:8	7:0
0x2638	fix_r2r_dly_count(RO)				fix_w2w_dly_count(RO)			
0x2640	fix_r2w_dly_count(RO)				fix_w2r_dly_count(RO)			
TST								
0x3000						lpbk_mode		

Offset	63:56	55:48	47:40	39:32	31:24	23:16	15:8	7:0
0x3178	obs[255:192] (RO)							
0x3180	obs[319:256] (RO)							
0x3188	obs[383:320] (RO)							
0x3190	obs[447:384] (RO)							
0x3198	obs[511:448] (RO)							
0x31a0	obs[575:512] (RO)							
0x31a8	obs[639:576] (RO)							
0x31b0					obs[671:640](RO)			
⋮								
0x3200								
0x3208								
0x3220	tud_i0							
0x3228	tud_i1							
0x3230	tud_o(RO)							
⋮								
0x3300	tst_300							
0x3308	tst_308							
0x3310	tst_310							
0x3318	tst_318							
0x3320	tst_320							
0x3328	tst_328							
0x3330	tst_330							
0x3338	tst_338							
0x3340	tst_340							
0x3348	tst_348							
0x3350	tst_350							
0x3358	tst_358							
0x3360	tst_360							
0x3368	tst_368							
0x3370	tst_370							
0x3378	tst_378							

13.3

13.3.1

Δ . h ك Init_start 0x010 Ω 0x2 ض Init_start
ً ╠ ì ك
ٮ DRAM Δ .

(1) pm_clk_sel_ckca غ pm_clk_sel_ds

(2) pm_phy_init_start 1 Δ . PHY

(3) DLL ش ٮ pm_dll_init_done 1

(4) ش pm_dll_lock_* pm_pll_lock_* ΐ 1

(5) pm_clken_*

(6) pm_init_start 1 ṗ └ ك Δ .

(7) ṗ └ ك Δ . ٮ pm_dram_init pm_cs_enable

13.3.2

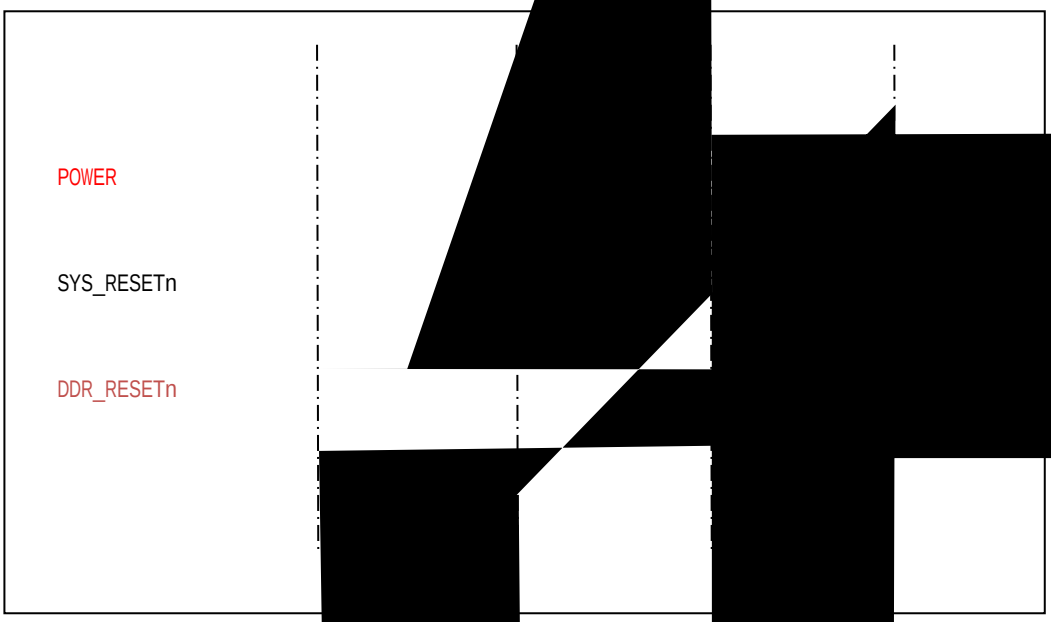
ض STR ٧ ٮ ض ٮ └ ً pad_reset_po 0x808
ك ≠ DDR_RESETn └ └

(1) reset_ctrl[1:0] == 2 ' b00 ً
└ ` ا DDR_RESETn ṗ

└ ك Δ .

(3) pm_pad_reset_o[1:0] == 2

DDR_RESETn



STR 2

STR 3

13.3.3 Leveling

Leveling DDR4

Write Leveling Read Leveling

Write Leveling Read Leveling

Read L DQS

GATE DQ

bit

13.3.3.1 Write Leveling

Write Leveling Ω DQS ă

(1) ă

(2) Dll_wrdqs_x x = 0 8 0x20

(3) Dll_wrdq_x x = 0 8 0x0

(4) Lvl_mode 2'b01

(5) Lvl_ready 1 Write Leveling

(6) Lvl_req 1

(7) Lvl_done 1 Write Leveling

(8) Lvl_resp_x 0 Dll_wrdq_x[6:0] dll_1xdly[6:0] 1 5-7 Lvl_resp_x 1 9 1 Dll_wrdq_x[6:0] dll_1xdly[6:0] 1 5-7 Lvl_resp_x 0 Dll_wrdq_x[6:0] dll_1xdly[6:0] 1 5-7 Lvl_resp_x 1 9

(9) Dll_wrdq_x dll_1xdly 0x40 Dll_wrdq_x dll_1xdly

(10) DIMM pm_dly_2x 0x0 pm_dly_2x 0x010101

(11) Lvl_mode 0x700 2'b00 Write Leveling

13.3.3.2 Gate Leveling

Gate Leveling ă DQS

(1) ă

(2) Write Leveling ă

(3) Dll_gate_x x = 0 8 0

(4) Lvl_mode 2'b10

(5) Lvl_ready 1 Gate Leveling

(6) Lvl_req 1

(7) Lvl_done 1 Gate Leveling

0 ↕

(4) Ω Mrs_req 0x1126 1 h DRAM ὖ MRS ث

(5) Mrs_done 0x1127 1 ↕ MRS ث ὖ ˜ ₹

0 ↕

(6)

(6) ك Lpbk_error 1 ں ˆ

Lpbk_* ك ₣ غ

0 ₣

13.3.8 ECC

ECC w ₇ ض 64 ˆ

Ecc_enable ₡

13- 3 1 ρ └ ₣

1 ρ └ ECC Mc1_ecc_set	0x0700	RW	1 ρ └ ECC [5:0] MC1 int_enable [8]: MC1 int_trigger [21:16]: MC1 int_vector(RO) h 7 [33:32]: MC1 ecc_enable ECC w [40]: MC1 rd_before_wr Ω w
	0x0708	RW	
1 ρ └ ECC Mc1_ecc_cnt	0x0710	RW	1 ρ └ ECC [7:0]: MC1 int_cnt ECC [15:8]: MC1 int_cnt_err(RO) ECC ₣ 7 [23:16]: MC1 int_cnt_fatal(RO) ECC ₣ 7
1 ρ └ ECC ₣ Mc1_ecc_cs_cnt	0x0718	RO	1 ρ └ ECC ₣ [7:0]: MC1 ecc_cnt_cs_0 CS0 ₣ ECC [15:8]: MC1 ecc_cnt_cs_1 CS1 ₣ ECC [23:16]: MC1 ecc_cnt_cs_2 CS2 ₣ ECC [31:24]: MC1 ecc_cnt_cs_3 CS3 ₣ ECC [39:32]: MC1 ecc_cnt_cs_4 CS4 ₣ ECC [47:40]: MC1 ecc_cnt_cs_5 CS5 ₣ ECC [55:48]: MC1 ecc_cnt_cs_6 CS6 ₣ ECC [63:56]: MC1 ecc_cnt_cs_7 CS7 ₣ ECC
1 ρ └ ECC Mc1_ecc_code	0x0720	RO	1 ρ └ ECC [7:0]: MC1 ecc_code_64 64 ECC ECC ρ w [41:32]: MC1 ecc_code_256 256 ECC ECC ρ w [52:48]: MC1 ecc_code_dir ρ ECC 7 ρ w [60:56]: MC1 ecc_data_dir ρ ECC 7 ρ w
1 ρ └ ECC ₣	0x0728	RO	1 ρ └ ECC ₣

خي ض ك Mc1_ecc_addr			[63:0]: MC1 ecc_addr ECC ₹ خي ض
1ˆ ṗ └ك ECC ₹ ك 0 Mc1_ecc_data0	0x0730	RO	1ˆ ṗ └ك ECC ₹ ك 0 [63:0]:Mc1_ecc_data0 ECC ₹ 64 ECC 256 ECC [63:0]
1ˆ ṗ └ك ECC ₹ ك 1 Mc1_ecc_data1	0x0738	RO	1ˆ ṗ └ك ECC ₹ ك 1 [63:0]:Mc1_ecc_data1 ECC ₹ 256 ECC [127:64]
1ˆ ṗ └ك ECC ₹ ك 2 Mc1_ecc_data2	0x0740	RO	1ˆ ṗ └ك ECC ₹ ك 2 [63:0]:Mc1_ecc_data2 ECC ₹ 256 ECC [191:128]
1ˆ ṗ └ك ECC ₹ ك 3 Mc1_ecc_data3	0x0748	RO	1ˆ ṗ └ك ECC ₹ ك 3 [63:0]:Mc1_ecc_data3 ECC ₹ 256 ECC [255:192]

14 HyperTransport

3A6000 HyperTransport

IO Cache Uncache

14.5.14 Cache IO DMA Cache

Cache ,

HyperTransport 16 3.2GHz

U

14.1

HT1.0/HT3.0

200/400/800/1600/2000/2400/3200MHz

HT3.0 8/16

PowerOK Rstn LDT_Stopn

14.1 HyperTransport

HyperTransport ,

HyperTransport

14- 1 Hyper

x01xxx	NPC or PC	Write	bit 5 0 - Nonposted 1 - Posted bit 2 0 – Byte 1 – Doubleword bit 1 Don ' t Care bit 0 Don ' t Care
01xxxx	NPC	Read	bit 3 Don ' t Care bit 2 0 – Byte 1 – Doubleword bit 1 Don ' t Care bit 0 Don ' t Care
110000	R	RdResponse	
110011	R	TgtDone	Ω
111010	PC	Broadcast	
111100	PC	FENCE	
111111	-	Sync/Error	Sync/Error

000000	-	NOP	
x01x0x	NPC or PC	Write	bit 5 0 - Nonposted 1 - Posted bit 2 0 – Byte 1 – Doubleword bit 0 0
010x0x	NPC	Read	bit 2 0 – Byte 1 – Doubleword bit 0 Don ' t Care
110000	R	RdResponse	
110011	R	TgtDone	Ω
111111	-	Sync/Error	

14.3 HyperTransport

HyperTransport 256 Fix Arbiter EOI U Ω 14.514.5.7

14.3.1 PIC

PIC PIC PIC PIC PIC PIC 4 U PIC 3A6000 HyperTransport 3 PIC Ω

256 h ضي U 4 ٦
h PIC └ ڪ ŭ ₣ U

14.3.2

HT └ ڪ ṗ h ٬P
HT └ ڪ ڪ № ŭ ’ HT ₇
₃ CPU № ŭ ڜ ẗ
ضي HT ڪ ṗ
⌠ HT └ ڪ h 0xefdfb000080 U
⌠ HT └ ڪ

14F3>3 48 ŧ ŧ > q ŧ Ó Yà

ضي 3A6000 I0 ˜ ₹ № ŭ
HT PIC ẗ Ω ڪ
ڪ ٬P ڪ ˜ № ŭ
I0 U HŦ- Q˜HĘ, ṗ ⌠ I0
ڪ 0x1800 ŭ ₇ ⌠
HT └ ڪ ڪ ŭ

14.4 HyperTransport

3A6000 كج HyperTransport o خي ضر o №

14- 5 HyperTransport o خي ضر

خي ضر	خي ضر		
0x0E00_0000_0000	0x0EFF_FFFF_FFFF	1 TB	HT o

ضي ' خي ضر o ع خي ضر

HyperTransport o ً آ آ خي ضر o

آ خي ضر آ 33.2 HyperTransport o ṗ 40 ضر

خي آ خي ضر o № خي

14- 6 3ً كج HyperTransport o ṗ خي ضر o №

خي ضر	خي ضر		
0x00_0000_0000	0xFC_FFFF_FFFF	1012 GB	MEM
0xFD_0000_0000	0xFD_0FFF_FFFF	256 MB	
0xFD_1000_0000	0xFD_F7FF_FFFF	3712 MB	
0xFD_F800_0000	0xFD_F8FF_FFFF	16 MB	
0xFD_F900_0000	0xFD_F90F_FFFF	1 MB	PIC ذ
0xFD_F910_0000	0xFD_F91F_FFFF	1 MB	
0xFD_F920_0000	0xFD_FAFF_FFFF	30 MB	
0xFD_FB00_0000	0xFD_FBFF_FFFF	16 MB	HT ك
0xFD_FC00_0000	0xFD_FDFF_FFFF	32 MB	I/O
0xFD_FE00_0000	0xFD_FFFF_FFFF	32 MB	HT
0xFE_0000_0000	0xFF_FFFF_FFFF	8 GB	

ŭ ج ⌡ HyperTransport
act_as_slave 1 ٧ ضي
ضي ضر ٥ ṗ
ٱ ٧
ج ∓

ضي ضر ٥ ṗ ∞ ٦ Ω
Post Write
Post Write HyperTransport ٧
Ω Ω ذ
HyperTransport
Ω ٧ ضي ٧ ك ⌊ h ŭ ∓ Ω
Post Write U ك Ω
ذ

ك ŭ
∓ ŭ
IO
∞ ٦ ṗ , HT ⌊ ك
ضي
Cache ج HyperTransport
ŭ
Ď

Post ٥
٥ 2 ṗ
14.5.12

˜ ŭ ٥
٥ 2 ṗ
14.5.13

	0x20				
	0x24				
	0x28	Cardbus CIS Pointer			
	0x2c	Subsystem ID		Subsystem Vendor ID	
	0x30	Expansion ROM Enable Address			
	0x34	Reserved			Capabilities Pointer
	0x38	Reserved			
	0x3c	Bridge Control		Interrupt Pin	Interrupt Line
Cap 0 PRI	0x40	Command		Capabilities Pointer	Capability ID
	0x44	Link Config 0		Link Control 0	
	0x48	Link Config 1		Link Control 1	
	0x4C	LinkFreqCap0		Link Error0/Link Freq 0	Revision ID
	0x50	LinkFreqCap1		Link Error1/Link Freq 1	Feature
	0x54	Error Handling		Enumeration Scratchpad	
	0x58	Reserved		Mem Limit Upper	Mem Enable Upper
Cap 1 Retry	0x60	Capability Type	Reserved	Capability Pointer	Capabiliter ID
	0x64	Status 1	Control 1	Status 0	Control 0
	0x68	Retry Count 1		Retry Count 0	
CAP 3	0x6C	Capability Type	Revision ID	Capability Pointer	Capabiliter ID
CAP 4 Interrupt	0x70	Capability Type	Index	Capability Pointer	Capabiliter ID
	0x74	Dataport			
	0x78	IntrInfo[31:0]			
	0x7C	IntrInfo[63:32]			
Int Vector	0x80	INT Vector[31:0]			
	0x84	INT Vector[63:32]			
	0x88	INT Vector[95:64]			
	0x8C	INT Vector[127:96]			
	0x90	INT Vector[159:128]			
	0x94	INT Vector[191:160]			

	0x98	INT Vector[223:192]			
	0x9C	INT Vector[255:224]			
	0xA0	INT Enable[31:0]			
	0xA4	INT Enable[63:32]			
	0xA8	INT Enable[95:64]			
	0xAC	INT Enable[127:96]			
	0xB0	INT Enable[159:128]			
	0xB4	INT Enable[191:160]			
	0xB8	INT Enable[223:192]			
	0xBC	INT Enable[255:224]			
CAP 5 Gen3	0xC0	Capability Type	Cap Enum/Index	Capability Pointer	Capabiliter ID
	0xC4	Global Link Training			
	0xC8	Transmitter Configuration 0			
	0xCC	Receiver Configuration 0			
	0xD0	Link Training 0			
	0xD4	Frequency Extension			
	0xD8	Transmitter Configuration 1			
	0xDC	Receiver Configuration 1			
	0xE0	Link Training 1			
	0xE4	BIST Control			

Enable	0x100	Device ID		Vendor ID	
	0x104	Status		Command	
	0x108	Class Code			Revision ID
	0x10c	BIST	Header Type	Latency Timer	Cache Line Size
	0x110				
	0x114				
	0x118				
	0x11c				
	0x120				
	0x124				
	0x128	Cardbus CIS Pointer			

	0x12c	Subsystem ID	Subsystem Vendor ID	
	0x130	Expansion ROM Enable Address		
	0x134	Reserved		Capabilities Pointer
	0x138	Reserved		
	0x13c	Bridge Control	Interrupt Pin	Interrupt Line
Receive Windows	0x140	HT RX Enable 0		
	0x144	HT RX Mask 0		
	0x148	HT RX Enable 1		
	0x14C	HT RX Mask 1		
	0x150	HT RX Enable 2		
	0x154	HT RX Mask 2		
	0x158	HT RX Enable 3		
	0x15C	HT RX Mask 3		
	0x160	HT RX Enable 4		
	0x164	HT RX Mask 4		
Header Trans	0x168	HT RX Header Trans		
	0x16C	HT RX EXT Header Trans		
Post Windows	0x170	HT TX Post Enable 0		
	0x174	HT TX Post Mask 0		
	0x178	HT TX Post Enable 1		
	0x17C	HT TX Post Mask 1		
Prefetchable Windows	0x180	HT TX Prefetchable Enable 0		
	0x184	HT TX Prefetchable Mask 0		
	0x188	HT TX Prefetchable Enable 1		
	0x18C	HT TX Prefetchable Mask 1		
Uncache Windows	0x190	HT RX Uncache Enable 0		
	0x194	HT RX Uncache Mask 0		
	0x198	HT RX Uncache Enable 1		
	0x19C	HT RX Uncache Mask 1		
	0x1A0	HT RX Uncache Enable 2		
	0x1A4	HT RX Uncache Mask 2		
	0x1A8	HT RX Uncache Enable 3		

	0x1AC	HT RX Uncache Mask 3
	0x1B0	HT RX P2P Enable 0
P2P	0x1B4	HT RX P2P Mask 0
Windows	0x1B8	HT RX P2P Enable 1
	0x1BC	HT RX P2P Mask 1
	0x1C0	APP Configuration 0
APP	0x1C4	APP Configuration 1
Config	0x1C8	RX Bus Value
	0x1CC	PHY status
	0x1D0	TX Buffer 0
	0x1D4	TX
Buffer		

	0x26C	HT TX POST ID WIN3
INT TRANS WINDOW	0x270	INT TRANS WIN lo
	0x274	INT TRANS WIN hi

ע í ב

14.5.1 Bridge Control

0x3C

0x00000000

O Bus Reset Control

14- 8 Bus Reset Control ע

	O				
31:23	Reserved 0	9	0x0		
22	Reset	1	0x0	R/W	L 0->1 HT_RSTn 0 1->0 HT_RSTn 1
21:0	Reserved	22	0x0		

14.5.2 Capability Registers

0x40

0x00006008

O Command Capabilities Pointer Capability ID

	Pointer				
7:0	Capability ID	8	0x08	R	HyperTransport capability ID

0x44

0x00112000

O Link Config Link Control

14- 10 Link Config Link Control ﻙ

	O				
					ΰ
					' U ╠
30:28	Link Width Out	3	0x0	R/W	Ώ ﻙ ﺽ HT Disconnect U
					000 8
					001 16
27	Reserved	1	0x0		
26:24	Link Width In	3	0x0	R/W	' U ╠ Ώ ﻙ ﺽ HT Disconnect U
23	Dw Fc out	1	0x0	R	ΰ ΐ
22:20	Max Link Width out	3	0x1	R	HT ΰ 16bits
19	Dw Fc In	1	0x0	R	ΐ
18:16	¢ î ¡				

7:0	Revision ID	8	0x60	R/W	˜	3.0

3A6000 ಶ ಶ ʻY

3A6000 ಶ ಶ

[0,4,8,12 l· l· 252] 0

[1,5,9,13 l· l· 253] 1

[2,6,10,14 l· l· 254] 2

[3,7,11,15 l· l· 255] 3

h ht_int_stripe_1 ³ ˜ ⌈

0x80

0x00000000

O HT h ক [31:0]

14- 20 HT h ক 1

	O				
31:0	Interrupt_case [31:0]	32	0x0	R/W	HT h ক [31:0]

0x84

0x00000000

O HT h ক [63:32]

14- 21 HT h ক 2

	O				
31:0	Interrupt_case [63:32]	32	0x0	R/W	HT h ক [63:32]

0x88

0x00000000

O HT h ক [95:64]

14- 22 HT h ক 3

	O				
31:0	Interrupt_case [95:64]	32	0x0	R/W	HT h ক [95:64]

0x8c

0x00000000

O HT h ক [127:96]

14- 23 HT h ক 4

O	

14.5.8

ლ ¨ 256 h ლ 1 0

↕

256 h ლ □ ⌈ □ ΐ

14.5.7

0xa0

0x00000000

O HT ლ [31:0]

14- 27 HT ლ 1

O					
31:0	Interrupt_mask [31:0]	32	0x0	R/W	H1

14- 30 HT ক 4

	O				
31:0	Interrupt_mask [127:96]	32	0x0	R/W	HT ক [127:96]

0xb0

0x00000000

O HT ক [159:128]

14- 31 HT ক 5

	O				
31:0	Interrupt_mask [159:128]	32	0x0	R/W	HT ক [159:128]

0xb4

0x00000000

O HT ক [191:160]

14- 32 HT ক 6

	O				
31:0	Interrupt_mask [191:160]	32	0x0	R/W	HT ক [191:160]

14.5.10

HT ك ض ي خ ث ٥

```
hit = ( BASE & MASK ) == ( ADDR & MASK )
addr_out_trans  n$
```

	O				
15:0	ht_rx_image0_mask[39:24]	16	0x0	R/W	HT خي ضر o 0 خي ضر [39:24]

0x148

0x00000000

O HT خي ضر o 1

14- 38 HT خي ضر o 1 كج

	O				
31	ht_rx_image1_en	1	0x0	R/W	HT خي ضر o 1 ~
30	ht_rx_image1_trans_en	1	0x0	R/W	HT خي ضر o 1 ~
29	ht_rx_image1_multi_node_en	1	0x0	R/W	HT خي ضر o 1 خي ضر

خي ضر [39:37]

	O				
					خي ضر [39:37] ⌠ [46:44]
28	ht_rx_image2_conf_hit_en	1	0x0	R/W	HT خي ضر o 2 ٦ ث خي ضر 0
25:0	ht_rx_image2_trans[49:24]	26	0x0	R/W	HT خي ضر o 2 U خي ضر [49:24]

0x154

0x00000000

O HT خي ضر o 2 خي

14- 41 HT خي ضر o 2 خي كج

	O				
31:16	ht_rx_image2_base[39:24]	16	0x0	R/W	HT خي ضر o 2 خي ضر خي [39:24]
15:0	ht_rx_image2_mask[39:24]	16	0x0	R/W	HT خي ضر o 2 خي ضر [39:24]

0x158

0x00000000

O HT خي ضر o 3

14- 42 HT خي ضر o 3 كج

	O				
31	ht_rx_image3_en	1	0x0	R/W	HT خي ضر o 3 ~
30	ht_rx_image3_trans_en	1	- ŧ		

	O				
31:16	ht_rx_image3_base[39:24]	16	0x0	R/W	HT خي ضر o 3 خي ضر خي [39:24]
15:0	ht_rx_image3_mask[39:24]	16	0x0	R/W	HT خي ضر o 3 خي ضر [39:24]

0x160

0x00000000

O HT خي ضر o 4

14- 44 HT خي ضر o 4 كج

	O				
31	ht_rx_image4_en	1	0x0	R/W	HT خي ضر o 4 ً
30	ht_rx_image4_trans_en	1	0x0	R/W	HT خي ضر o 4 ً
29	ht_rx_image4_multi_node_en	1	0x0	R/W	HT خي ضر o 4 خي ضر خي ضر [39:37] ⌡ [46:44]
28	ht_rx_image4_conf_hit_en	1	0x0	R/W	HT خي ضر o 4 ٦ ث خي ضر 0
25:0	ht_rx_image4_trans[49:24]	26	0x0	R/W	HT خي ضر o 4 U خي ضر [49:24]

0x164

0x00000000

O HT خي ضر o 4 خي

14- 45 HT خي ضر o 4 خي كج

	O				
31:16	ht_rx_image4_base[39:24]	16	0x0	R/W	HT خي ضر o 4 خي ضر خي [39:24]
15:0	ht_rx_image4_mask[39:24]	16	0x0	R/W	HT خي ضر o 4 خي ضر [39:24]

14.5.11

HT ٩

0x168

0x00000000

O خي ضر

14- 46 خي ضر كج

	O				
					0xFD_FE000000 U
31	ht_rx_header_trans_ext	1	0x1	R/W	ﺨﻲﺿ type1 24 ⌈ 28 EXT HEADER
30	ht_rx_header_trans_en				

O		

ACC o)

29:23

0x00000000

O HT POST خي ضر o 2 ṗ

14- 52 HT POST خي ضر o 2 ṗ

	O				
31	ht_post2_en	1	0x0	R/W	HT POST خي ضر o 2 ˜
30	ht_split2_en	1	0x0	R/W	HT ´ (CPU uncache ACC o)
29:23	Reserved	14	0x0		
15:0	ht_post2_trans[39:24]	16	0x0	R/W	HT POST خي ضر o 2 U خي ضر [39:24]

0x3A4

0x00000000

O HT POST خي ضر o 2 خي ṗ

14- 53 HT POST خي ضر o 2 خي ṗ

	O				
31:16	ht_post2_base[39:24]	16	0x0	R/W	HT POST خي ضر o 2 خي ضر خي [39:24]
15:0	ht_post2_mask[39:24]	16	0x0	R/W	HT POST خي ضر o 2 خي ضر [39:24]

0x3A8

0x00000000

O HT POST خي ضر o 3 ṗ

14- 54 HT POST خي ضر o 3 ṗ

	O				
31	ht_post3_en	1	0x0	R/W	HT POST خي ضر o 3 ˜
30	ht_split3_en	1	0x0	R/W	HT ´ (CPU uncache ACC o)
29:16	Reserved	14	0x0		
15:0	ht_post3_trans[39:24]	16	0x0	R/W	HT POST خي ضر o 3 U خي ضر [39:24]

0x3Ac

0x00000000

O HT POST خي ضر o 3 خي ṗ

14- 55 HT POST خي ضر o 3 خي ṗ

	o				
31:16	ht_post3_base[39:24]	16	0x0	R/W	HT POST خي ضر o 3 خي ضر خي [39:24]
15:0	ht_post3_mask[39:24]	16	0x0	R/W	HT POST خي ضر o 3 خي ضر [39:24]

14.5.13

خي ضر o ث 14.5.10

o خي ضر AXI ⌠ خي ضر ضي o ŭ ĭ CACHE

ŭ HT ì ŭ CACHE ŭ HT ٧ عج

ث ↕ عج

0x180

0x00000000

O HT ˆ ŭ ضر خي o 0 ṗ

14- 56 HT ˆ ŭ ضر خي o 0 ṗ

	o				
31	ht_prefetch0_en	1	0x0	R/W	HT ˆ ŭ ضر خي o 0 ˆ
30:16	Reserved	15	0x0		
15:0	ht_prefetch0_trans[39:24]	16	0x0	R/W	HT ˆ ŭ ضر خي o 0 U ضر خي [39:24]

0x184

0x00000000

O HT ˆ ŭ ضر خي o 0 خي ṗ

14- 57 HT ˆ ŭ ضر خي o 0 خي ṗ

14- 58 HT ً خي ضر ٌّ ٥ 1 ڤ

o				
31	ht_prefetch1_en	1	0x0	R/W HT ً ضر ٌّ etch

o							
28	ht_uncache0_conf_hit_en	1	0x0	R/W	HT	uncache	خي ضر ٦ 0 ٥ خي ضر
					ث		
25:0	ht_uncache0_trans[49:24]	26	0x0	R/W	HT	uncache	خي ضر ٥ 0 che a

14- 63 HT Uncache خيضر ٥ 1 خي ṗ

	o		

31:16

31	ht_uncache3_en	1	0x0	R/W	HT	uncache خي ض ٥ 3 ~
30	ht_uncache3_trans_en	1	0x0	R/W	HT	

3A6000 ಶ ಶ

					0 -> 1 LDT DISCONNECT ة HT LDT_REQ_n
28	Ldt Req Gen	1	0x0	R/W	0 P 1 0 -> 1 h ü ₹ Ω ً ة ـ
27	rx sample en	1	0x0	R/W	cad غ ctl ض 0x1c8 ك
26	Dword Write	1	0x1	R/W	32/64/128/256 MEM

					111 0
15	[illegible]h	1	0x	R/W	CRC ŭ
14:12	Crc Int route	[illegible]	[illegible]	R/W	CRC
11	Reserved				
10	ht int 8 bit	1	0x0	R/W	8 3 ĺ h ٪
9:8	ht_int_stripe	2	0x0	R/W	0x0 ht_int_stripe_1 0x1 ht_int_stripe_2 0x2 ht_int_stripe_4 ‰ ì h ⌠ ك h ´ SMI NMI INIT INTTH, ش
4:0	Interrupt Index	5	0x0	R/W	

					1	5	CTL1
0							

14.5.18 PHY

PHY

0x1C0C

0x83308000

O PHY

14- 75 PHY

	O					
31:29	Reserved	3	0x0	R		
28	dll locked hi	1	0x0	R	8	DLL
27	dll locked lo	1	0x0	R	8	DLL
26	cdr locked hi	1	0x0	R	8	CDR
25	cdr locked lo	1	0x0	R	8	CDR
24	phase locked	1	0x0	R		
23:20	phy state	4				

14- 76 ث ڻ ك

o						
31:24	B_CMD_txbuffer	8	0x0	R	ڻ	B ث
23:16	R_CMD_txbuffer	8	0x0	R	ڻ	R ث
15:8	NPC_CMD_txbuffer	8	0x0	R	ڻ	NPC， ثp

7:0	PC_DATA_txbuffer	8	0x0	R	ὃ PC

14.5.21

ὃ ლ HT ᒪლ ὃ ‖ ᛘ ⁞

 ὃ

0x1D8

0x00000000

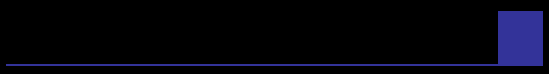
O ὃ ლ

14- 78 ὃ ლ

	O

ß

7:4	NPC_CMD_txadj	4	0x0	R/W



14- 83 Training 2 ש

	o				
31:0	T2 time	32	0x7fffff	R/W	Training 2 ש

14.5.27 Training 3

HyerTransport 3.0 Training 3 ש

HyperTransport3.0 1/4

0x1F0

O Training 3 ש

14- 84 Training 3 ש

o		
31:0 T3 time	32	

HyperTransport 3.0:

PHY_LINK_CLK 100MHz × div_loop /div_refc /phy_div

PLL ضي ' system clk 33M 30us ~ ضي

ك Ω

ضي 3C5000 HT_CORE_CLK 'P L NODE №

L

0x1F4

0x00000000

O ك

14- 85 ك

	O				
31	Reserved	1	0x0	R/W	
30 26	Soft_phy_hi_div	5	0x0	R/W	PHY №
25	Reserved	1	0x0	R/W	
24 20	Soft_phy_lo_div	5	0x0	R/W	PHY №
19 17	Reserved	3	0x0	R/W	
16 8	Soft_div_loop	9	0x0	R/W	PLL ṗ
7 4	Soft_div_refc	4	0x0	R/W	PLL ṗ №
3	Locked	1	0x0	R	
2	Bypass ht core	1	0x0	R/W	ă L ك
1	Soft cofig enable	1	0x0	R/W	1 ' b0 1 ' b1
0	Reserved	1	0x0	R/W	

14.5.29 PHY

L PHY ٧ ŭ غ ٧ ă

0x1F8

0x00000000

O PHY ٧ L ك

14- 86 ٧ L ك

	O				

31	Tx_scanin_en	1	0x0	R/W	TX Ꭹ
30	Rx_scanin_en	1	0x0	R/W	RX Ꭹ
27:24	Tx_scanin_ncode	4	0x0	R/W	TX Ꭹ ncode
23:20	Tx_scanin_pcode	4	0x0	R/W	TX Ꭹ pcode
19:12	Rx_scanin_code	8	0x0	R/W	RX Ꭹ

14.5.30 PHY

PHY ᵀ ắ └ლ 8bit └ლ

PHY ẹ PHY №≠ └ლ └ └ლ 1 16bit └ლ

ẹ PHY ắ └ლ └

0x1FC

0x83308000

O PHY ლ

14- 87 PHY ლ

	O				
31	Rx_ckpll_term	1	0x1	R/W	PLL ⌠ RX
30	Tx_ckpll_term	1	0x0	R/W	PLL ⌠ TX
29	Rx_clk_in_sel	1	0x0	R/W	PAD PAD HT1 ⌟ CLKPAD: 1 ' b0 1 ' b1 PLL
28	Rx_ckdll_sell	1	0x0	R/W	DLL 1 ' b0 PLL 1 ' b1
27:26	Rx_ctle_bitc	2	0x0	R/W	PAD EQD
25:24	Rx_ctle_bitr	2	0x3	R/W	PAD EQD
23:22	Rx_ctle_bitlim	2	0x0	R/W	PAD EQD └
21	Rx_en_ldo	1	0x1	R/W	LDO └ 1 ' b0 LDO 1 ' b1 LDO

	O				
31:16	Rx_wait_time	16	0x0	R/W	RX ৸ Δ
15:0	Tx_wait_time	16	0x0	R/W	TX ৸ Δ

0x248

0x00000000

O LDT ৸ 2

14- 90 LDT ৸ 2

	O				
31:30	Reserved	16	0x0	R/W	
29:0	rx lane ts 0	16	0x0	R/W	

0x24C

0x00000000

O LDT ৸ 3

14- 91 LDT ৸ 3

	O				
31:30	Reserved	16	0x0	R/W	
29:0	rx lane ts 1	16	0x0	R/W	

0x250

0x00000000

O LDT ৸ 4

14- 92 LDT ৸ 4

	O				
31:30	Reserved	16	0x0	R/W	
29:0	rx lane ts 2	16	0x0	R/W	

0x254

0x00000000

O LDT ৸ 5

14- 93 LDT ৵ 5

	O				
31:22	Reserved	10	0x0	R/W	
21:18	wait ctl	4	0x0	R/W	
17:0	phase lock	18	0x0	%IJ	

					o ID MASK
15:0	HT TX POST ID1 BASE	16	0x0	R/W	AXI ID ث POST o ID BASE

0x268

0x00000000

O HT TX POST ID WIN2

14- 97 HT TX POST ID WIN2

	O				
31:16	HT TX POST ID2 MASK	16	0x0	R/W	AXI ID ث POST o ID MASK
15:0	HT TX POST ID2 BASE	16	0x0	R/W	AXI ID ث POST o ID BASE

0x26C

0x00000000

O HT TX POST ID WIN3

14- 98 HT TX POST ID WIN3

	O				
31:16	HT TX POST ID3 MASK	16	0x0	R/W	AXI ID ث POST o ID MASK
15:0	HT TX POST ID3 BASE	16	0x0	R/W	AXI ID ث POST o ID BASE

14.5.36 Bist

ك HT ض bist

0x340

0x00000010

O bist L ك

14- 102 bist L ك

	O				
31:5	Reserved	27	0x0	R/W	
4	bist_resetn	1	0x1	R/W	bist ~
3	bist_fail	1	0x0	R/W	bist ₹
2	prbs_lpbk_en	1	0x0	R/W	prbs
1	prbs_32	1	0x0	R/W	prbs_32
0	bist_mode	1	0x0	R/W	bist

0x344

0x00000000

O bist ك 0

14- 103 bist ك 0

	O				
31:8	bist_error_bit0	24	0x0	R/W	bist ₹
7:0	bist_error_cnt0	8	0x0	R/W	bist ₹ bit

0x348

0x00000000

O bist ك 1

14- 104 bist ك 1

	O				
31:8	bist_error_bit1	24	0x0	R/W	bist ₹
7:0	bist_error_cnt1	8	0x0	R/W	bist ₹ bit

14.5.37 LDO

৵ PHY ṗ LDO U

0x350

0xBFA38783

O LDO ৵

14- 105 LDO ৵

	O	

14.5.40 Unitid

id HT Ü unitid

0x360

0x00000000

O unitid L ر 0

14- 108 unitid L ر 0

	O				
31:21	Reserved	11	0x0	R/W	
23:16	unit_id0	5	0x0	R/W	0 o unitid
15:8	axi2unitid0_mask	8	0x0	R/W	0 o id
7:0	axi2unitid0_base	8	0x0	R/W	0 o id

7:0	axi2unitid2_base	8	0x0	R/W	2 ˆ o id خي

0x36C

0x00000000

O unitid L ر 3

14- 111 unitid L ر 3

	O				
31:21	Reserved	11	0x0	R/W	
23:16	unit_id3	5	0x0	R/W	3 ˆ o ﻫ unitid
15:8	axi2unitid3_mask	8	0x0	R/W	3 ˆ o id
7:0	axi2unitid3_base	8	0x0	R/W	3 d" ﷺ " ﷺ "

J

19:15	LC_VTH1_CTRL_N	5	0x18	R/W	
14:10	LC_VTH1_CTRL_P	5	0x18	R/W	
9:5	LC_VTH2_CTRL_N	5	0x18	R/W	
4:0	LC_VTH2_CTRL_P	5	0x18	R/W	

14.5.44 PLL

৸ PLL U ĭ ἅ

0x37C

0x0000600f

O PLL ৸

14- 115 PLL ৸

	o			

o خي ضر HT ⌡ خي ضر ضي o خي ضر ث POST

NONPOST L ═ ì ṗ ث o

0x1C0[17:16] ì

ì 0 3

0x380

0x00000000

O HT o 0

14- 116 HT o 0 كج

	o				
31	ht_rx_prior0_en	1	0x0	R/W	HT o 0 ˜
30	ht_rx_prior0_post_en	1	0x0	R/W	HT o 0 POST
29	ht_rx_prior0_nonpost_en	1	0x0	R/W	HT o 0 NONPOST
1:0	ht_rx_prior0	2	0x0	R/W	HT o 0 ث U

0x384

0x00000000

O HT o 0 خي

14- 117 HT o 0 خي كج

	o				
31:16	ht_rx_prior0_base[39:24]	16	0x0	R/W	HT o 0 خي خي ضر [39:24]
15:0	ht_rx_prior0_mask[39:24]	16	0x0	R/W	HT o 0 خي ضر [39:24]

0x1B8

0x00000000

O HT o 1

14- 118 HT o 1 كج

	o				
31	ht_rx_prior1_en	1	0x0	R/W	HT o 1 ˜
30	ht_rx_prior1_post_en	1	0x0	R/W	HT o 1 POST
29	ht_rx_prior1_nonpost_en	1	0x0	R/W	HT o 1 NONPOST
1:0	ht_rx_prior1	2	0x0	R/W	HT o 1 ث U

0x1BC

0x00000000

O HT o 1 خي

14- 119 HT o 1 خي كح

	O				
31:16	ht_rx_prior1_base[39:24]	16	0x0	R/W	HT o 1 خي ضخي خي [39:24]
15:0	ht_rx_prior1_mask[39:24]	16	0x0	R/W	HT o 1 خي ضخي [39:24]

14.5.46

خي ضخي o ث 14.5.10

خي ضخي o HT ⌡ خي ضخي 0xFD_0xxx_xxxx ضي

ث خي ضخي o ~ L

0x3C0

0x00000000

O HT o 0

14- 120 HT o 0 كح

	O				
31	ht_rx_ir0_en	1	0x0	R/W	HT o 0 ~

0x3C4

0x00000000

O HT o 0 خي

14- 121 HT o 0 خي كح

	O				
31:16	ht_rx_ir0_base[39:24]	16	0x0	R/W	HT o خي ضخي خي [39:24]
15:0	ht_rx_ir0_mask[39:24]	16	0x0	R/W	HT o خي ضخي [39:24]

14.6 HyperTransport

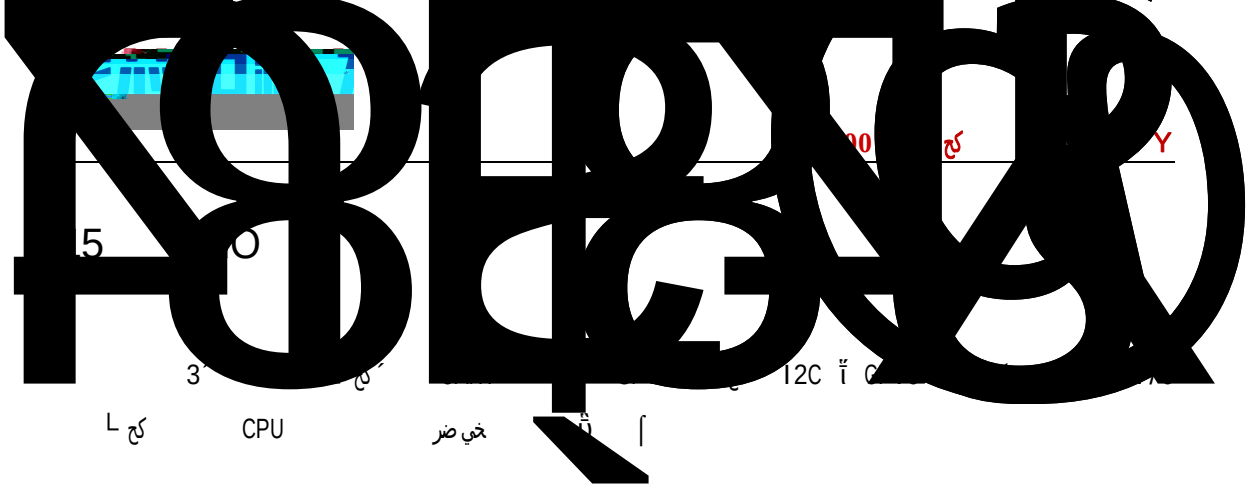
HyperTransport o ٦ PCI ٦

خي ضر HT ↓ ₹ 6 -14 ض أ ٓ ٦

مخ 0xFD_FE00_0000 0xFD_FFFF_FFFF HT ٦ ض 3A6000

Type 0:

Type 1:



15 O

3 I2C

CPU

15.1 UART

UART

/

16

FIFO

NS16550A

UART

UART1 GPIO

UART0 0x1FE001E0

UART1 0x1FE001E8

UART 0x1FE00100(UART0) 0x1FE00110(UART1)

TFC RFC

15.1.1 DA

15.1.2 IER

O ς

ς [7 0]

0x01

0x00

	O			
7:4	Reserved	4	RW	
3	IME	1	RW	Modem ‘0’ – ˜ ‘1’ –
2	ILE	1	RW	ς ‘0’ – ˜ ‘1’ –
1	ITxE	1	RW	ς ‘0’ – ˜ ‘1’ –
0	IRxE	1	RW	 ‘0’ – ˜ ‘1’ –

15.1.3 IIR

O ς

ς [7 0]

0x02

0xc1

	O			
7:4	Reserved	4	R	
3:1	II	3	R	
0	INTp	1	R	

L w

Bit 3	Bit 2	Bit 1				L
0	1	1	1st		₣	LSR
0	1	0	2nd	⌠	FIFO ⌠ trigger	FIFO trigger

1	1	0	2nd	ض FIFO	FIFO
				ض 4	ṗ
				ً	غ Ω
0	0	1	3rd	ك	Ω ⌈ THR
				ك	IIR
0	0	0	4th	Modem	

				‘0’ –
5	spb	1	RW	‘0’ – ‘1’ – LCR[4] 1 ↕ غ 0 LCR[4] 0 ↕ غ 1
4	eps	1	RW	‘0’ – ضي 1 ´ غ ‘1’ – ضي 1
3	pe	1	RW	‘0’ – ‘1’ – ضي ∓ ↕ ∞
2	sb	1	RW	‘0’ – 1 ‘1’ – ضي 5 1.5 ĩ 2
1:0	bec	2	RW	‘00’ – 5 ‘01’ – 6 ‘10’ – 7 ‘11’ – 8

15.1.6 MODEM MCR

O Modem L كح

كح [7 0]

0x04

0x00

O				
7:5	Reserved	3	W	
4	Loop	1	W	عج L ‘0’ – ‘1’ – عج

	O			
				ر ï DTR : DSR RTS : CTS Out1 : RI Out2 : DCD
3	OUT2	1	W	عجـ ضي ⌈ DCD
2	OUT1	1	W	عجـ ضي ⌈ RI
1	RTSC	1	W	RTS ˜ L
0	DTRC	1	W	DTR ˜ L

15.1.7 LSR

O ر

ر [7 0]

0x05

0x00

	O			
7	ERROR	1	R	‘ 1 ’ –
				‘ 0 ’ –
6	TE	1	R	‘ 1 ’ – FIFO ؛ ر

3	FE	1	R	‘1’ – ‘0’ F–
2	PE	1	R	‘1’ – ╠ ‘0’ –
1	OE	1	R	‡ ‘1’ – ‡ ‘0’ – ‡
0	DR	1	R	‘0’ – ضي FIFO ‘1’ – ضي FIFO

ك LSR[4:1] غ LSR[7] LSR[6:5]ضي FIFO Ω

LSR[0] ↕ FIFO ∞

15.1.8 MODE8

15.1.9 FIFO RFC

O FIFO

৸ [7 0]

0x08

0x00

O	
7:0	RFC 3

0x02

0x00

	O			
7:0	D_DIV	8	RW	№ ك №

15.1.12

FIFO ك RFC ˆ CPU FIFO CPU
ˆ ض ⌠ U ŭ CPU UART Z
ŭ FIFO ك TFC ˆ CPU ŭ FIFO CPUˆ ض
ŭ FIFO ₣ ╠ ŭ CPU UART ŭ Z
№ ك 3 ٧ № ك ═ ⌠
ă 100MHz 16 'P ي № № ك ك
MSB غ LSB № 256 № ك D_DIV

15.2 SPI

SPI └ ك ĭ

ĭ □ o

⌠ 4 ĭ

ŭ ₣

ĭ ‖ ك

غ ˆ

ˆ ض SPI └

SPI Ω⌐

Dual/Quad mode SPI flash

SPI └ ك ك ضر خي خي 0x1FE001F0

15- 1 SPI └ ك خي ضر №

ضر خي O	مذ خي ضر	
SPI Boot	0x1C00_0000-0x1CFF_FFFF	16MByte
SPI Memory	0x1D00_0000-0x1DFF_FFFF	16MByte
SPI Register	0x1FE0_01F0-0x1FE0_01FF	16Byte

SPI Boot خي ضر Ω¯ ك خي ضر

SPI Memory ˜ CPU

15.2.1 SPCR

O L ك

ك [7 0]

0x00

0x10

	O			
7	Spie	1	RW	₹ ˜
6	spe	1	RW	˜
5	Reserved	1	RW	
4	mstr	1	RW	master 1
3	cpol	1	RW	
2	cpha	1	RW	1 ↕ ï 0 ↕ □
1:0	spr	2	RW	sclk_o № sper spre

15.2.2 SPSR

O ك

ك [7 0]

0x01

0x05

	O			
7	spif	1	RW	1 Ώ 1 ↕
6	wcol	1	RW	Ώ ك ₹ 1 ₹ , Ώ 1 ↕
5:4	Reserved	2	RW	
3	wffull	1	RW	Ώ ك 1
2	wfempty	1	RW	Ώ ك 1
1	rffull	1	RW	ك 1
0	rfempty	1	RW	ك 1

15.2.3 TxFIFO

O ر

ر [7 0]

0x02

0x00

	O			
7:0	Tx FIFO	8	W	ر

15.2.4 SPER

O ر

ر [7 0]

0x03

0x00

	O			
7:6	icnt	2	RW	ضي U ₣ ˜ 00 – 1 01 - 2 10 - 3 11 - 3
5:2	Reserved	4	RW	
1:0	spre	2	RW	Spr №

№

spre	00	00	00	00	01	01	01	01	10	10	10	10
spr	00	01	10	11	00	01	10	11	00	01	10	11
№	2	4	16	32	8	64	128	256	512	1024	2048	4096

15.2.5 SFC_PARAM

O SPI Flash ǎ L ر

ر [7 0]

0x04

0x21

	O			
7:4	clk_div	4	RW	№ № {spre,spr}
3	dual_io	1	RW	I/O
2	fast_read	1	RW	
1	burst_en	1	RW	spi flash
0	memory_en	1	RW	spi flash csn[0]

15.2.6 SFC_SOFTCS

O SPI Flash

ك ك s> c ك

15.2.11 1 BUF1

O	SPI Flash	ক 1
ক	[7 0]	
	0x0b	
	0x00	

O	

0x0e

0x00

	o			
7:0	time2	8	RW	ث 8

15.2.15 SPI

SPI (dual mode) quad mode

SPI flash dual_io SPI

quad_io SPI BIOS

U

SPI FLASH

(dummy clocks) SPI FLASH

(0x8-0xe)

1. CMD 0x9 h SPI FLASH ث
2. SPI FLASH ث

TIMER0-TIMER2(0xc-0xe) 0

3. h SPI FLASH

BUF0-BUF1(0xa-0xb) h SPI FLASH

4. CTRL[7 1] CTRL[1](nbmode)

CTRL[7:4](nbyte)

5. CTRL[0]

FLASH

15.3 I2C

I2C

I2C

I2C SDA SCL

400kbps

3A6000 I2C

ض ṗ ك ® ṻ ṗ

خي ك SLV_CTRL[6:0]

I2C0 ك└ ك ك خي ضخي 0x1FE00120

I2C1 ك└ ك ك خي ضخي 0x1FE00130

ك ṗ ί

15.3.1 PRERlo

O № ك ك

ك [7 0]

0x00

0xff

O				
7:0	PRERlo	8	RW	№ ك 8

15.3.2 PRERhi

O № ك ك

ك [7 0]

0x01

0xff

O				
7:0	PRERhi	8	RW	№ ك 8

№ ك prescale LPB PCLK clock_aSCL

∓ clock_s ↕ ˜

Prcescale = clock_a/(4*clock_s)-1

15.3.3 CTR

O └ ك

ك [7 0]

0x02

0x20

O	

7	EN	1	RW	شجِ 1 , 0 № كج
6	IEN	1	RW	1 ↕
5	MST_EN	1	RW	شجِ 0 slave 1 master
4:0	Reserved	5	RW	

15.3.4 TXR

O ŭ كج

كج [7 0]

0x03

0x00

O				
7:1	DATA	7	W	ŭ
0	DRW	1	W	Ω خي ضر

15.3.5 RXR

O كج

كج [7 0]

0x03

0x00

O				
7:0	RXR	8	R	U ⌠

15.3.6 CR

O ث كج

كج [7 0]

0x04

0x00

O				
7	STA	1	W	START ؆
6	STO	1	W	STOP ؆
5	RD	1	W	؆
4	WR	1	W	Ω ؆
3	ACK	1	W	؆
2:1	Reserved	2	W	
0	IACK	1	W	؆

ض I2C ŭ U ـ عج ‘ 0 ’ bit 3 1

└ كح ŭ ack ĭ ŭ ack

15.3.7 SR

O كح

كح [7 0]

0x04

0x00

O				
7	RxACK	1	R	⌈ 1 ⌈ 0 ⌈
6	Busy	1	R	I2c 1 ض 0
5	AL	1	R	I2C ˇ I2C └ 1
4:2	Reserved	3	R	
1	TIP	1	R	 1 ض 0
0	IF	1	R	٣ كح ŭ 1

15.3.8 SLV_CTRL

O L كج

كج [7 0]

0x07

0x00

O				
7	SLV_EN	1	WR	MST_EN 0 ˜ ṗ
6 0	SLV_ADDR	7	WR	I2C خي ضر ˜

15.4 AVS

AVS L كج كج ضر خي خي 0x1FE00160

15- 2 AVS L كج ضر خي №

O ضر خي	مخ ضر خي	
AVS Register	0x1FE0_0160-0x1FE0_016F	16B

15.4.1 CSR

O L كج

كج [31 0]

0x0

0x0

	O			
31	resyn	1	RW	1 ضي ╠ □ 0 ↕ □ 0
30:29	mask_ack	2	RW	Ω 1 mask alert_ack
28	mask_i	1	RW	1 mask alert_i
27	mask_s	1	RW	1 mask alert_s
26	mask_c	1	RW	1 mask alert_c
25	mask_a	1	RW	1 mask alert_a
24	rx_ctrl	1	RW	L كج 1 ضي AVS 0 ضي AVS

				0
23:20	rx_delay	4	RW	1 ۱ U 2 ۱ U 0
19:17	clk_div	3	RW	№ 0x0 № 0x1 ضم№ 0x2 № 0x3 ٧ Έ№ 0x4 ٧ № 0x5 Έ ٧ضم№ №
16	Dmux	1	RW	1 Ἰ عج 0 Ἰ 0
15:0	reserved	16	—	—

15.4.2 Mreg

O ἅ L ك

ك [31 0]

0x4

0x0

O				
31	TX_EN	1	RW	Ώ 1 AVS
30:29	cmd	2	RW	0x0 Ώ 0x1 Ώ ۱ 0x2 0x3 Ώ cmd 0
28	group	1	RW	0 AVS ٦ ≠ 1 L ٨ ڍ ≠
27:24	cmd_type	4	RW	0x0 ۱ ث 1LSB=1mv 0x1 ۱ ث cmd_data 0x2 ث ٧ 0x3 ث ٧ 0x4 ۱ ث ٧ Ώ 0x5 w ث 0x6~0xd 0xe ث 0xf ث
23:20	rail_sel	4	RW	۱ 0xf ↕
19:4	cmd_data	16	RW	Ώث ۱ ث ˜ 0 ث 1
3:0	reserved			

3A6000